1MHz, High-Efficiency, Step-Up Converter for 2 to 10 White LEDs

Features

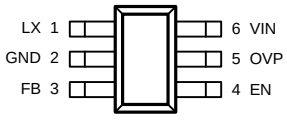
- **Wide Input Voltage from 2.5V to 6V**
- **0.3V Reference Voltage**
- **Fixed 1MHz Switching Frequency**
- **High Efficiency up to 88%**
- **100Hz to 100kHz PWM Brightness Control Frequency**
- **Open-LED Protection**
- **Under-Voltage Lockout Protection**
- **Over-Temperature Protection**
- **<1µA Quiescent Current during Shutdown**
- **SOT-23-6 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **White LED Display Backlighting**
- **Cell Phone and Smart Phone**
- **PDA, PMP, MP3**
- **Digital Camera**

Pin Configuration

SOT-23-6 Top View



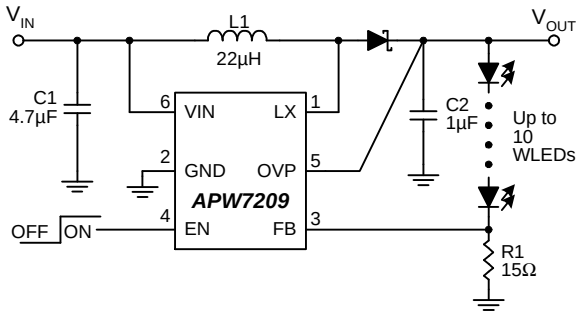
General Description

The APW7209 is a current-mode and fixed frequency boost converter with an integrated N-FET to drive up to 10 white LEDs in series.

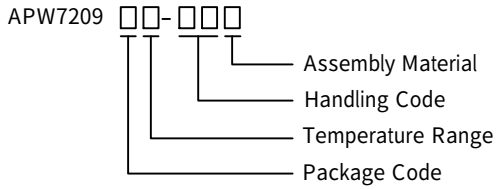
The series connection allows the LED current to be identical for uniform brightness. Its low on-resistance of N-FET and low feedback voltage reduce power loss and achieve high efficiency. Fast switching frequency(1MHz typical) allows using small-size inductor and both of input and output capacitors. An over voltage protection function, which monitors the output voltage via OVP pin, stops switching of the IC if the OVP voltage exceeds the over voltage threshold. An internal soft-start circuit eliminates the inrush current during start-up.

The APW7209 also integrates under-voltage lockout, over-temperature protection, and current limit circuits to protect the IC in abnormal conditions.The APW7209 is available in a SOT-23-6 package.

Simplified Application Circuit



Ordering and Marking Information



Package Code
C : SOT-23-6
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
L : Lead Free Device
G : Halogen and Lead Free Device

APW7209 CI: W09X

X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 7	V
	FB, EN to GND Voltage	-0.3 ~ V_{IN}	V
V_{LX}	LX to GND Voltage	-0.3 ~ 42	V
V_{OVP}	OVP to GND Voltage	-0.3 ~ 42	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance. SOT-23-6	250	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.5~ 6	V
C_{IN}	Input Capacitor	4.7 or higher	µF
C_{OUT}	Output capacitor	0.68 or higher	µF
L1	Inductor	6.8 ~ 47	µH
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit for further information.

Electrical Characteristics

(Refer to figure 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 3.6V, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.)

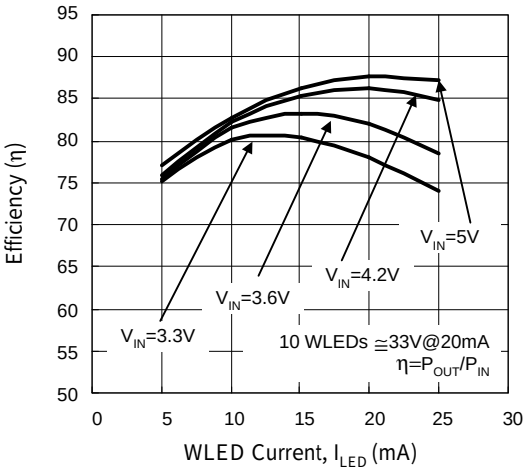
Symbol	Parameter	Test Conditions	APW7209			Unit
			Min.	Typ.	Max.	
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range	T_A = -40 ~ 85°C, T_J = -40 ~ 125°C	2.5	-	6	V
I_{DD1}	Input DC bias current	V_{FB} = 0.4V, no switching	70	100	130	µA
I_{DD2}		FB = GND, switching	-	1	2	mA
I_{SD}		EN = GND	-	-	1	µA
UNDER VOLTAGE LOCKOUT						
	UVLO Threshold Voltage	V_{IN} Rising	2.0	2.2	2.4	V
	UVLO Hysteresis Voltage		50	100	150	mV
REFERENCE AND OUTPUT VOLTAGES						
V_{REF}	Regulated Feedback Voltage	T_A = 25°C	0.285	0.3	0.315	V
		T_A = -40 ~ 85°C (T_J = -40 ~ 125°C)	0.276	-	0.324	
I_{FB}	FB Input Current		-50	-	50	nA
INTERNAL POWER SWITCH						
F_{SW}	Switching Frequency	FB=GND	0.8	1.0	1.2	MHz
R_{ON}	Power Switch On Resistance		-	0.6	-	Ω
I_{LIM}	Power Switch Current Limit		0.7	0.9	1.2	A
	LX Leakage Current	V_{EN}=0V, V_{LX}=0V or 5V, V_{IN} = 5V	-1	-	1	µA
D_{MAX}	LX Maximum Duty Cycle		92	95	98	%
OUTPUT OVER VOLTAGE PROTECTION						
V_{OVP}	Over Voltage Threshold	V_{OVP} rising	-	40	-	V
	OVP Hysteresis		-	3	-	V
	OVP Leakage Current	V_{OVP} =40V	-	50	-	µA
ENABLE AND SHUTDOWN						
V_{TEN}	EN Voltage Threshold	V_{EN} Rising	0.4	0.7	1	V
	EN Voltage Hysteresis		-	0.1	-	V
I_{LEN}	EN Leakage Current	V_{EN}= 0~5V, V_{IN} = 5V	-1	-	1	µA
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over-Temperature Protection (Note 4)	T_J Rising	-	150	-	°C
	Over-Temperature Protection Hysteresis (Note 4)		-	40	-	°C

Note 4: Guaranteed by design, not production tested.

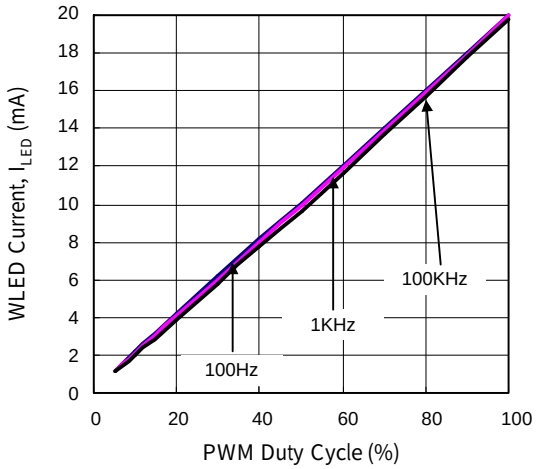
Typical Operating Characteristics

(Refer to figure 1 in the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, 10WLEDs unless otherwise specified)

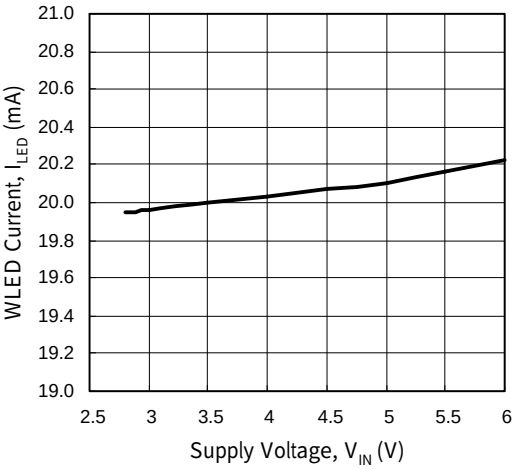
Efficiency vs. WLED Current



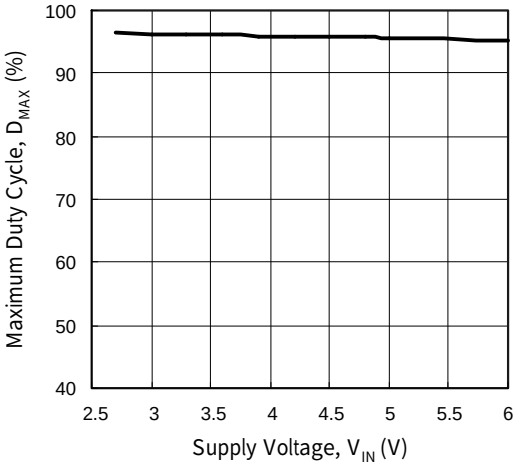
WLED Current vs. PWM Duty Cycle



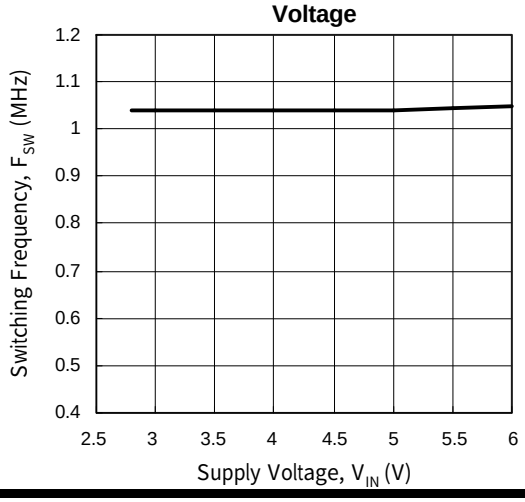
WLED Current vs. Supply Voltage



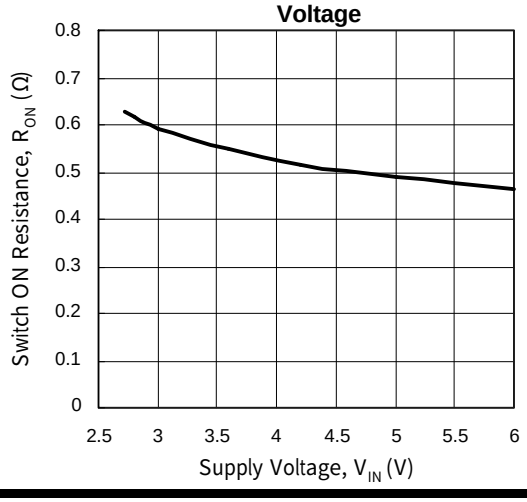
Maximum Duty Cycle vs. Supply Voltage



Switching Frequency vs. Supply Voltage



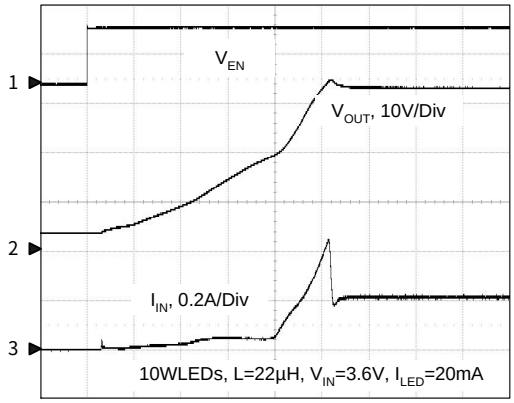
Switch ON Resistance vs. Supply Voltage



Operating Waveforms

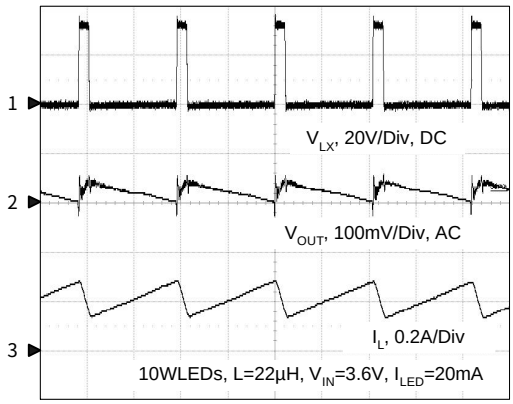
(Refer to the application circuit in the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, 10WLEDs unless otherwise specified)

Start-up



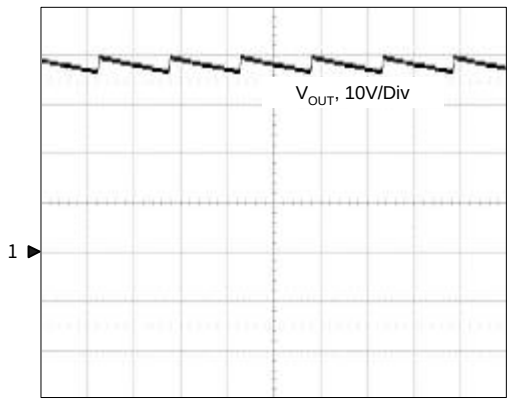
CH1: V_{EN}, 1V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: I_{IN}, 0.2A/Div, DC
Time: 0.5ms/Div

Normal Operating Waveform



CH1: V_{LX}, 20V/Div, DC
CH2: V_{OUT}, 100mV/Div, AC
CH3: I_L, 0.2A/Div, DC
Time: 500ns/Div

Open-LED Protection

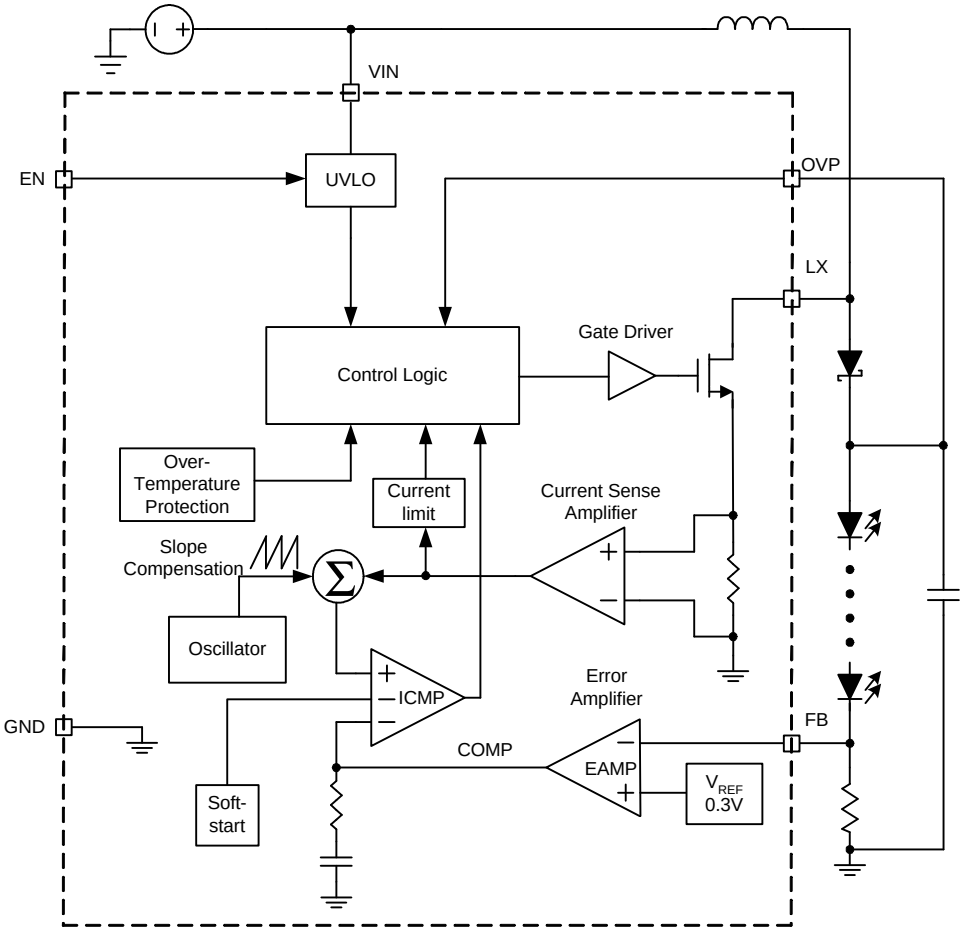


CH1: V_{OUT}, 10V/Div, DC
Time: 20ms/Div

Pin Description

PIN NO.	NAME	FUNCTION
1	LX	Switch pin. Connect this pin to inductor/diode here.
2	GND	Power and signal ground pin.
3	FB	Feedback Pin. Reference voltage is 0.3V(typical). Connect this pin to cathode of the lowest LED and current-sense resistor (R1). Calculate resistor value according to R1=0.3V/I_{LED}.
4	EN	Enable Control Input. Forcing this pin above 1.0V enables the device, or forcing this pin below 0.4V to shut it down. In shutdown, all functions are disabled to decrease the supply current below 1μA. **Do not leave this pin floating.**
5	OVP	Over Voltage Protection Input Pin. OVP is connected to the output capacitor of the converter.
6	VIN	Main Supply Pin. Must be closely decoupled to GND with a 4.7μF or greater ceramic capacitor.

Block Diagram



Typical Application Circuits

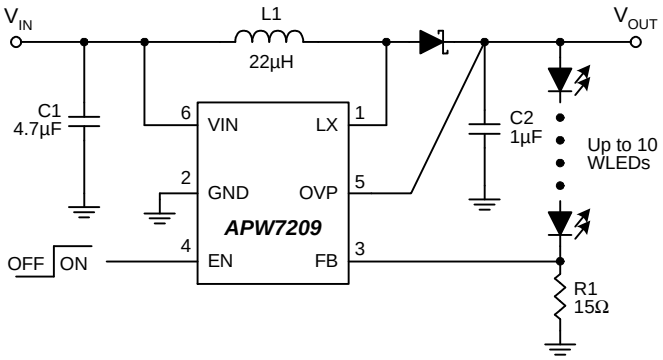


Figure 1. Typical 10 WLEDs Application

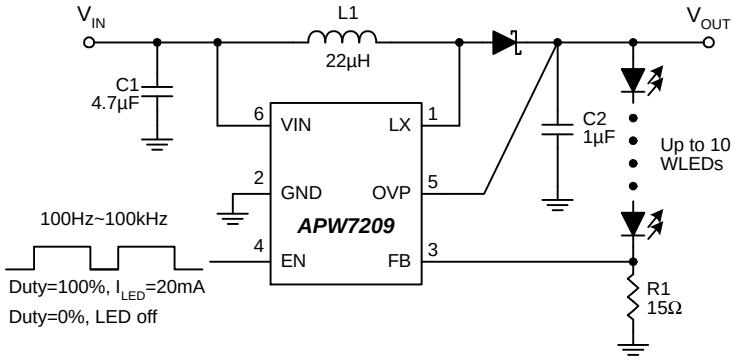
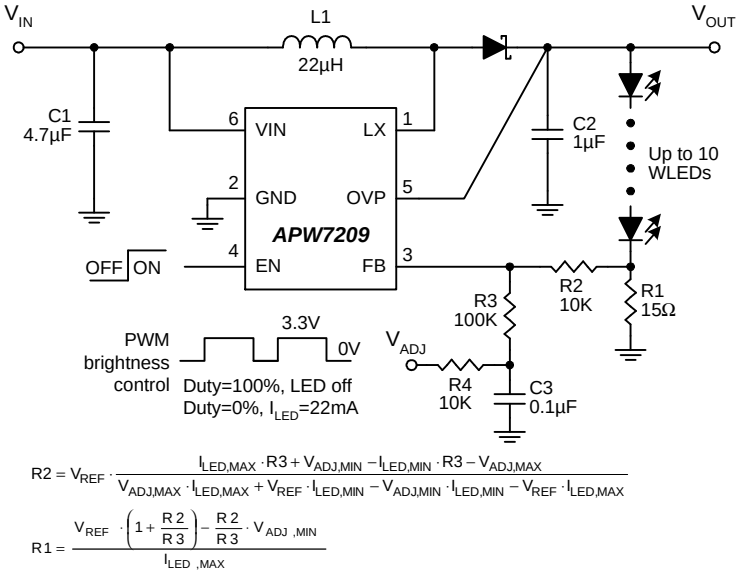


Figure 2. Brightness control by using a PWM signal applied to EN



$$R2 = V_{REF} \cdot \frac{I_{LED,MAX} \cdot R3 + V_{ADJ,MIN} - I_{LED,MIN} \cdot R3 - V_{ADJ,MAX}}{V_{ADJ,MAX} \cdot I_{LED,MAX} + V_{REF} \cdot I_{LED,MIN} - V_{ADJ,MIN} \cdot I_{LED,MIN} - V_{REF} \cdot I_{LED,MAX}}$$

$$R1 = \frac{V_{REF} \cdot \left(1 + \frac{R2}{R3}\right) - \frac{R2}{R3} \cdot V_{ADJ,MIN}}{I_{LED,MAX}}$$

Figure 3. Brightness control using a filtered PWM signal

Function Description

Main Control Loop

The APW7209 is a constant frequency current-mode switching regulator. During normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external current-sense resistor connected between cathode of the lowest LED and ground allows the EAMP to receive a current feedback voltage V_{FB} at FB pin. When the LEDs voltage increases to cause the LEDs current to decrease, it causes a slightly decrease in V_{FB} relative to the 0.3V reference, which in turn causes the COMP voltage to increase until the LEDs current reaches the set point.

VIN Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold (2.2V rising, typical) to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

Soft-Start

The APW7209 has a built-in soft-start to control the N-channel MOSFET current rise during start-up. During soft-start, an internal ramp voltage, connected to one of the inverting inputs of the comoarator ICMP, raise up to replace the output voltage of error amplifier until the ramp voltage reaches the V_{COMP}.

Current-Limit Protection

The APW7209 monitors the inductor current, flowing through the N-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the APW7209 from damages in overload conditions.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7209. When the junction temperature exceeds 150°C, a thermal sensor turns off the power MOSFET, allowing the device to cool. The thermal sensor allows the converter to start a soft-start process and regulate the LEDs current again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Enable/Shutdown

Driving EN to ground places the APW7209 in shutdown mode. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescnet supply current reduces to 1μA maximum.

This pin also could be used as a digital input allowing brightness controlled by using a PWM signal with frequency from 100Hz to 100kHz. The 0% duty cycle of PWM signal corresponds to zero LEDs current and 100% corresponds to full one.

Open-LED Protection

In driving LED applications, the feedback voltage on FB pin falls down if one of the LEDs, in series, is failed. Meanwhile, the converter unceasingly boosts the output voltage like a open-loop operation. Therefore, an over-voltage protection (OVP), monitoring the output voltage via OVP pin, is integrated into the chip to prevent the LX and the output voltages from exceeding their maximum voltage ratings. When the voltage on the OVP pin rises above the OVP threshold (40V, typical), the converter stops switching and prevents the output voltage from rising. The converter can work again when the falling OVP voltage falls below the OVP voltage threshold.

Application Information

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the ripple of the input current drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller when an input capacitor with larger capacitance is used. For reliable operation, it is recommended to select the capacitor with maximum voltage rating at least 1.2 times of the maximum input voltage. The capacitors should be placed close to the VIN and GND.

Inductor Selection

Selecting an inductor with low dc resistance reduces conduction losses and achieves high efficiency. The efficiency is moderated whilst using small chip inductor which operates with higher inductor core losses. Therefore, it is necessary to take further consideration while choosing an adequate inductor. Mainly, the inductor value determines the inductor ripple current: larger inductor value results in smaller inductor ripple current and lower conduction losses of the converter. However, larger inductor value generates slower load transient response. A reasonable design rule is to set the ripple current, ΔI_L, to be 30% to 50% of the maximum average inductor current, $I_{L(AVG)}$. The inductor value can be obtained as below,

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT}-V_{IN}}{F_{SW}\times I_{OUT(MAX)}} \times \frac{\eta}{\left(\frac{\Delta I_L}{I_{L(AVG)}}\right)}$$

where

V_{IN} = input voltage

V_{OUT} = output voltage

F_{SW} = switching frequency in MHz

I_{OUT} = maximum output current in amp.

η = Efficiency

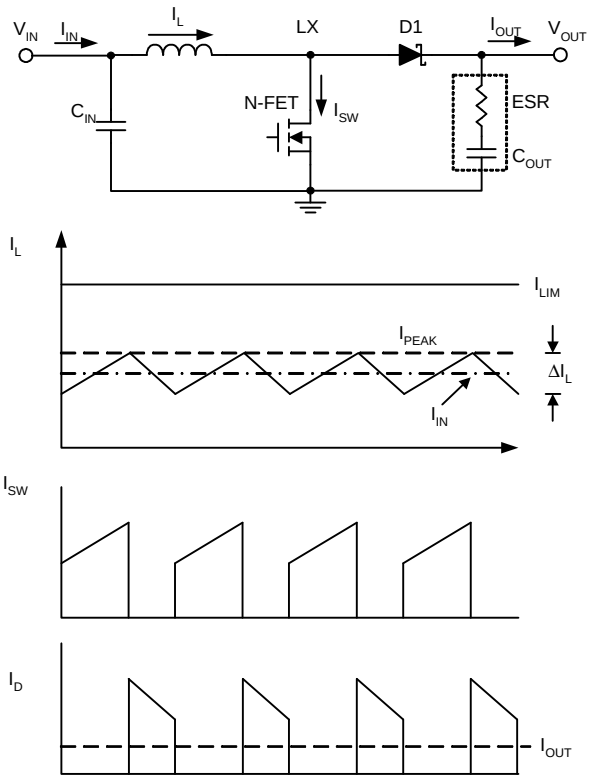
$\Delta I_L / I_{L(AVG)}$ = inductor ripple current/average current (0.3 to 0.5 typical)

To avoid saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)}\times V_{OUT}}{V_{IN}\times \eta}$$

The peak inductor current is calculated as the following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2}\cdot\frac{V_{IN}\cdot(V_{OUT}-V_{IN})}{V_{OUT}\cdot L\cdot F_{SW}}$$



Output Capacitor Selection

The current-mode control scheme of the APW7209 allows the usage of tiny ceramic capacitors. The higher capacitor value provides good load transient response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{COUT} \approx \frac{I_{OUT}}{C_{OUT}}\times\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}\times F_{SW}}\right)$$

$$\Delta V_{ESR} \approx I_{PEAK}\times R_{ESR}$$

where I_{PEAK} is the peak inductor current.

Application Information (Cont.)

Output Capacitor Selection (Cont.)

For ceramic capacitor application, the output voltage ripple is dominated by the ΔV_{COUT}. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

Diode Selection

To achieve high efficiency, a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter.

Setting the LED Current

In figure 1, the converter regulates the voltage on FB pin, connected with the cathod of the lowest LED and the current-sense resistor R1, at 0.3V (typical). Therefore, the current (I_{LED}), flowing via the LEDs and the R1, is calculated by the following equation:

$$I_{LED} = \frac{0.3V}{R1}$$

Recommended Inductor Selection

Designator	Manufacturer	Part Number	Inductance (µH)	Max DCR (ohm)	Saturation Current (A)	Dimensions L x W x H (mm^3)
L1	GOTREND	GTSD-53-470	47	0.35	0.62	5 x 5 x 2.8
L1	GOTREND	GTSD-32-220	22	0.59	0.52	3.85 x 3.85 x 1.8

Recommended Capacitor Selection

Designator	Manufacturer	Part Number	Capacitance (µF)	TC Code	Rated Voltage (V)	Case size
C1	Murata	GRM188R60J475KE19	4.7	X5R	6.3	0603
C2	Murata	GRM21BR71H105KA12	1.0	X7R	50	0805

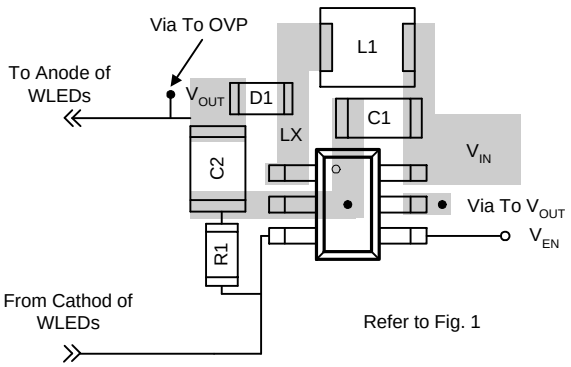
Recommended Diode Selection

Designator	Manufacturer	Part Number	Maximum average forward rectified current (A)	Maximum repetitive peak reverse voltage (V)	Case size
D1	Zowie	MSCD106	1.0	60	0805

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

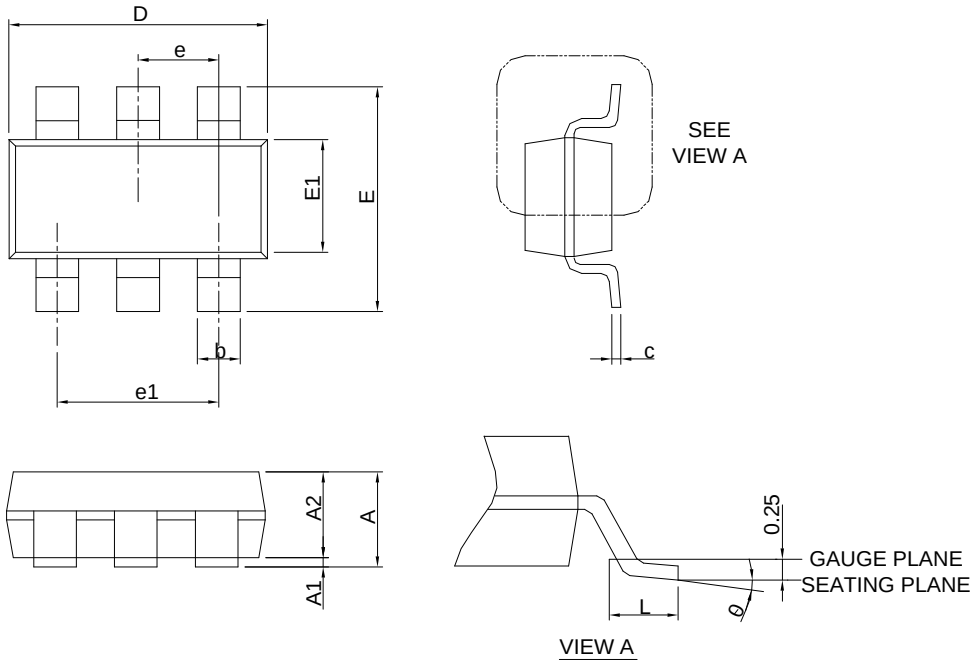
1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor with VIN and GND pins by short and wide tracks without using any vias for filtering and minimizing the input voltage ripple.
2. The inductor should be placed as close as possible to the LX pin to minimize length of the copper tracks as well as the noise coupling into other circuits.
3. Since the feedback pin and network is a high impedance circuit, the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or track to minimize noise coupling into this circuit.
4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.



Optimized APW7209 Layout

Package Information

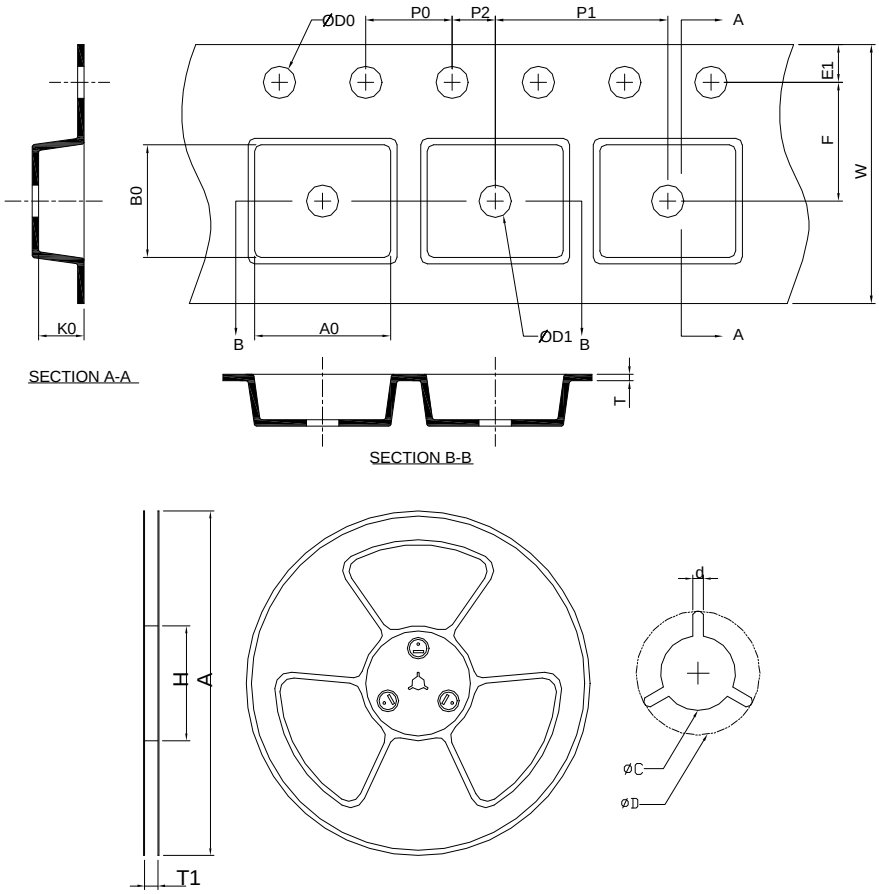
SOT-23-6



SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



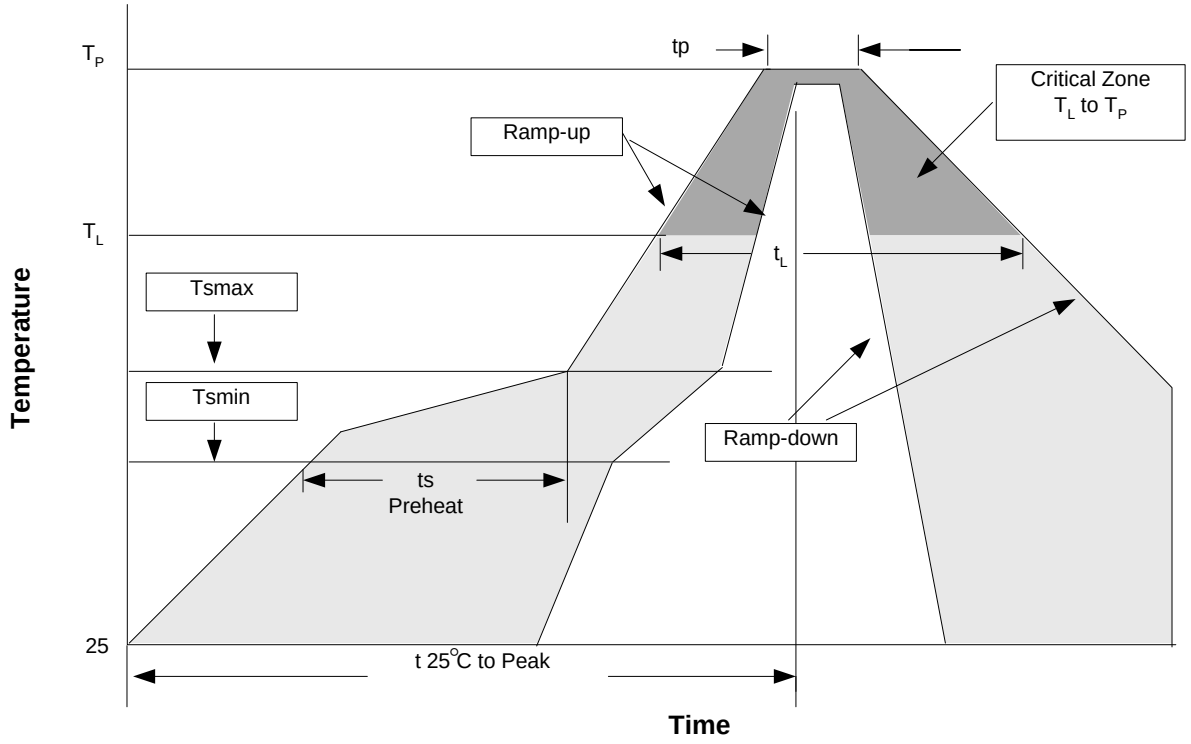
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOT-23-6	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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