SPECIFICATIONS
FOR
LCM+CTP+HDMI Module

MODULE No:	KD055HDFIA001-C001A_HDMI
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2019.07.08	V1.0	ALL	First version

Contents

1. Scope

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit,HDMI board and back-light unit. The resolution of a 5.5'TFT-LCD contains 720x1280 pix els, and can display up to 65K/262K/16.7M colors.

1.1 Basic Description

General Information Items	Specifications	Unit	Note
	Main Panel		
Display area(AA)	68.04(H)*120.96(V) (5.5inch)	mm	-
CTP View area	68.84(H)*121.76(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	720(RGB)*1280	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.0945(H)*0.0945(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9881C	-	-
CTP Driver IC	GT911		
Operating temperature	-20～+70	℃	
Storage temperature	-30～+80	℃	
LCM+CTP Luminance	310nits (Typ.)		
CTP Interface	Mirco-USB		
CTP Firmware Version	KD055HDFIA001-C001A CTP_V01		
CTP and LCM Bonding	Tape Bonding	-	-
Touch Cover Thickness	1.1mm with chemical strengthening		
Touch Point	Five points and Gestures		
Video Input	HDMI		
HDMI it Firmware Version	KD055HDFIA001-C001A _HDMI_V01		

1.2 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		86.04		mm	-
	Vertical(V)		144.96		mm	-
	Depth(D)		4.75		mm	-
Weight			122		g	-

1.3 Recommended Resolution

Recommended Resolution	720(RGB)*1280 @55~60 Hz

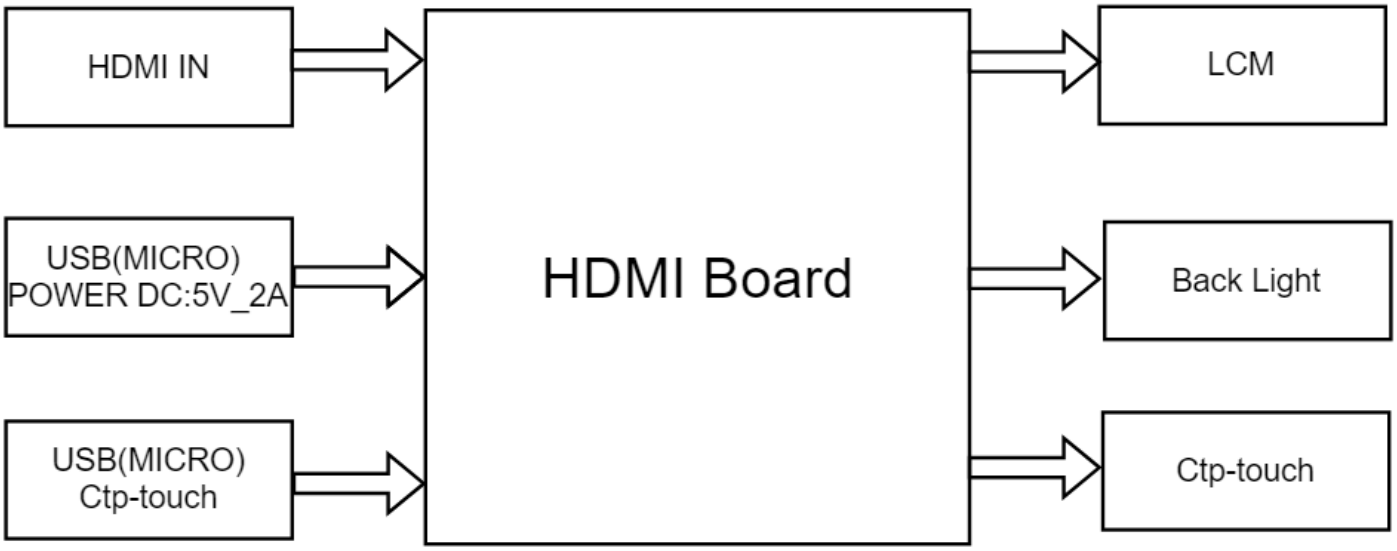
1.4 Plug & Play

DDC2B /VESA Standard

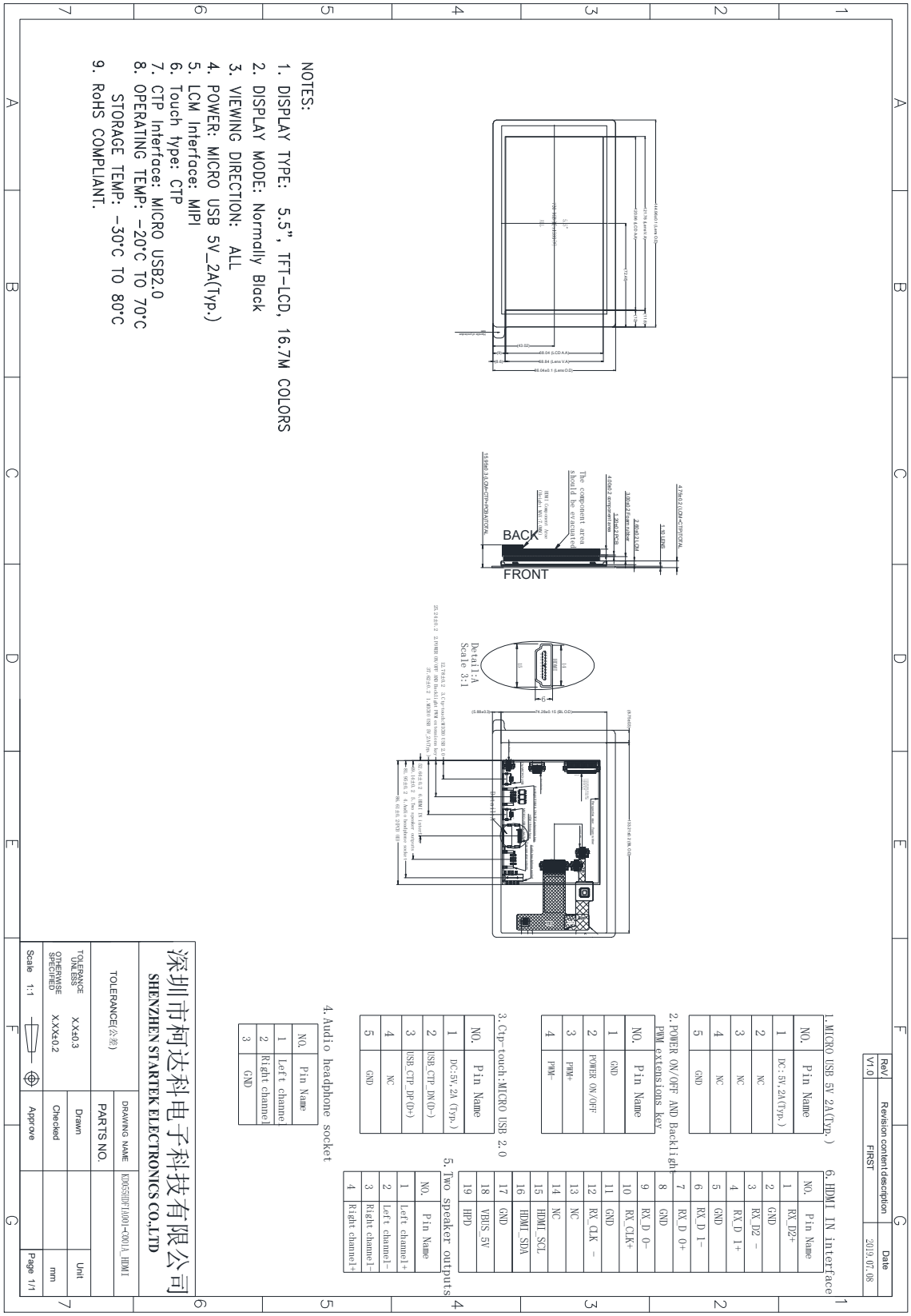
1.5 Power Supply Rating

Power Consumption	2.8W Watt (Typ.)
MICRO USB DC POWER	5V 2A(Typ.)

1.6 Block Diagram



1.7 Outline Dimension

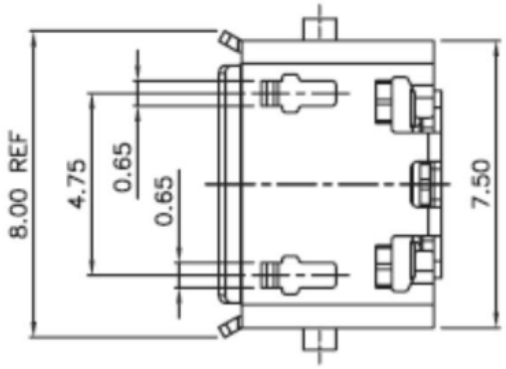


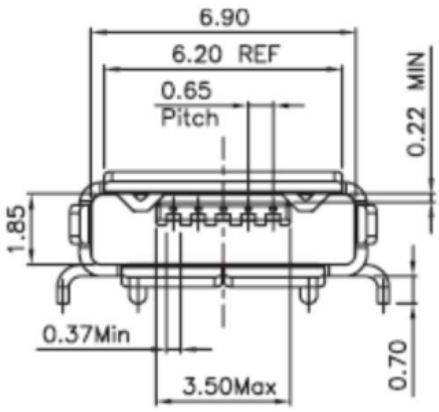
2. Input Terminal Pin Assignment

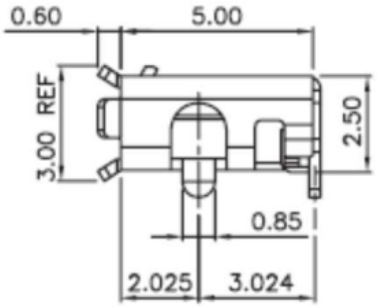
2.1 MICRO USB 5V_2A(Typ.) PIN Definition & Signal Connector

NO.	SYMBOL	DISCRIPTION	I/O
1	DC:5V,2A(Typ.)	Supply voltage(5.0V,2A Typ.).	P
2	NC	No Connection.	
3	NC	No Connection.	
4	NC	No Connection.	
5	GND	Ground.	P

Note: Mirco-USB Connector Dimension:



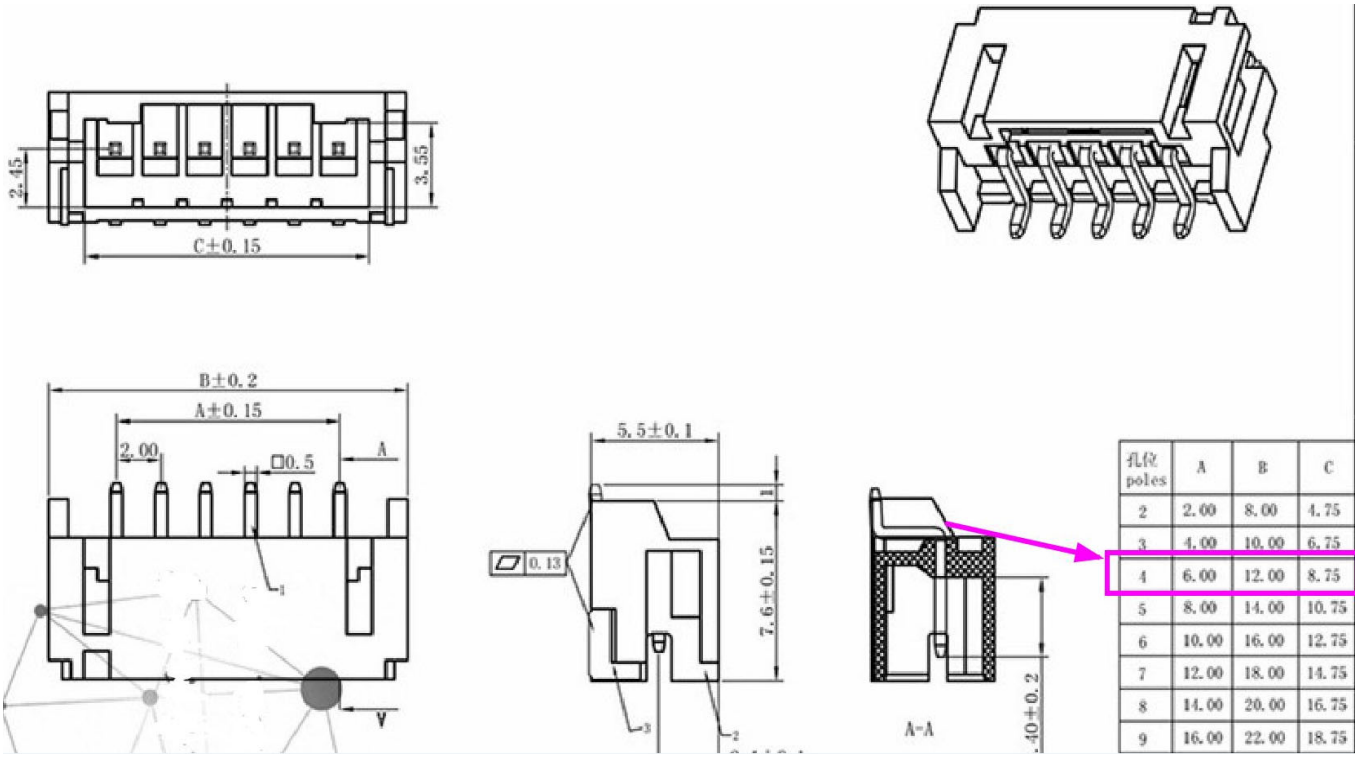




2.2 POWER ON/OFF AND Backlight PWM extensions key PIN Definition & Signal Connector

note: SMT PH2.0mm spacing connector 4p

NO.	SYMBOL	DISCRIPTION
1	GND	Ground
2	POWER ON/OFF	ON/OFF KEY
3	PWM+	The backlight brightness of each button is increased by one level until the maximum brightness reaches (9 level).
4	PWM-	The backlight brightness of each button is reduced by one evel until the lowest brightness reaches (level 9).

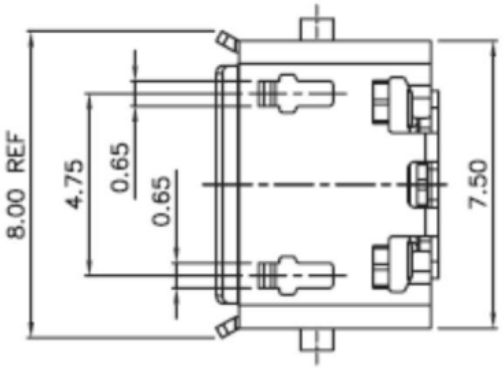


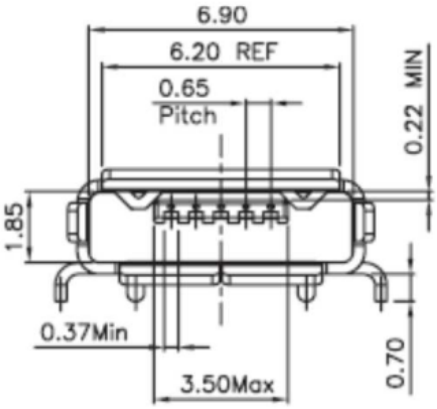
孔位 poles	A	B	C
2	2.00	8.00	4.75
3	4.00	10.00	6.75
4	6.00	12.00	8.75
5	8.00	14.00	10.75
6	10.00	16.00	12.75
7	12.00	18.00	14.75
8	14.00	20.00	16.75
9	16.00	22.00	18.75

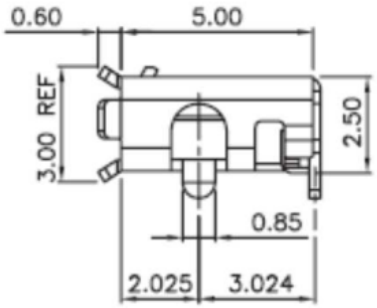
2.3 CTP: MICRO USB PIN Definition & Signal Connector

NO.	SYMBOL	DISCRIPTION	I/O
1	DC:5V,2A(Typ.)	Supply voltage(5.0V,2A Typ.).	P
2	USB_CTP_DN(D-)	USB data negative analog input.	I/O
3	USB_CTP_DP(D+)	USB data positive analog input.	I/O
4	NC	No Connection.	I
5	GND	Ground.	P

Note: Mirco-USB Connector Dimension:

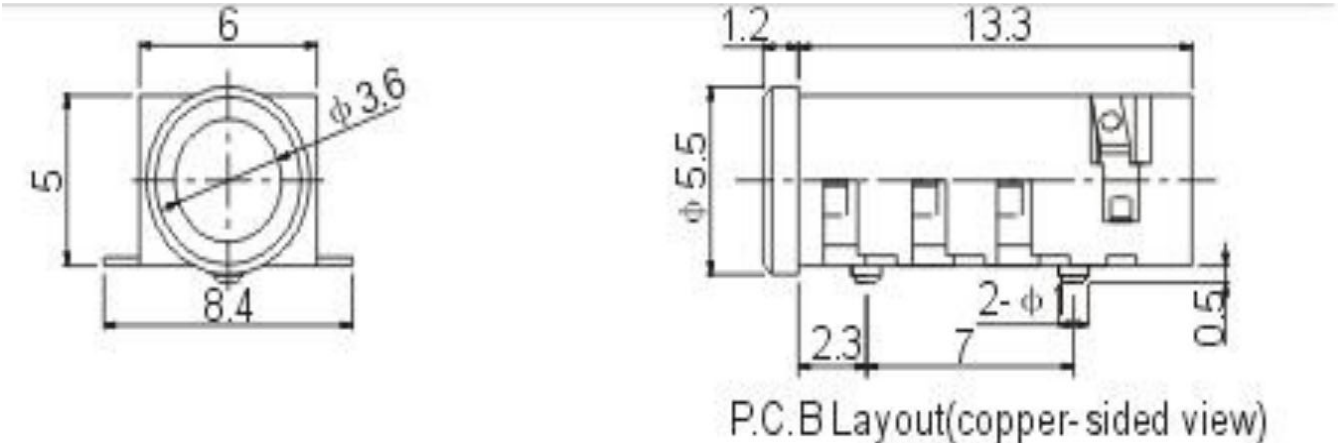






2.4 Audio headphone socket PIN Define & Input Signal Connector

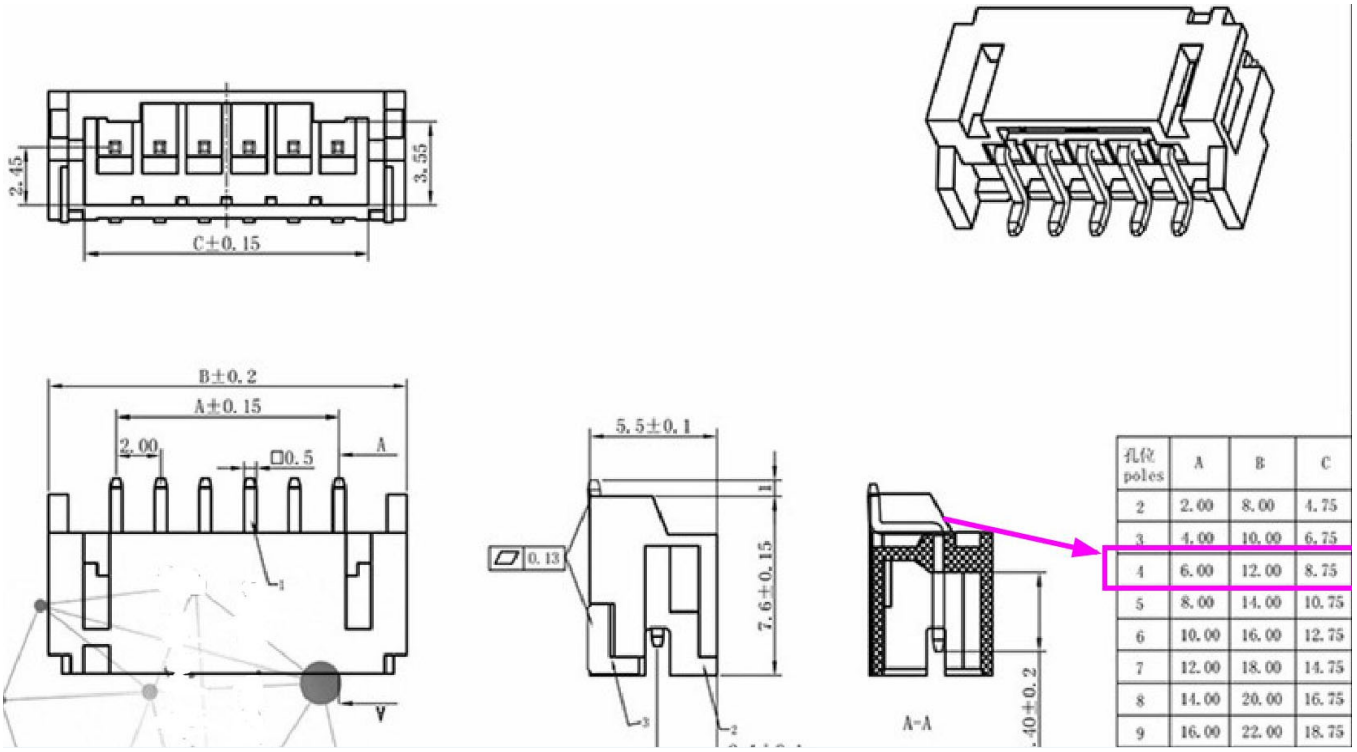
NO.	SYMBOL	DISCRIPTION
1	Left channel	Audio output left channel
2	Right channel	Audio output right channel
3	GND	Ground
4	GND	Ground



2.5 Two speaker outputs PIN Define & Input Signal Connector

note: SMT PH2.0mm spacing connector 4p

NO.	SYMBOL	DISCRIPTION
1	Left channel+	Audio output left channel
2	Left channel-	
3	Right channel-	Audio output right channel
4	Right channel+	

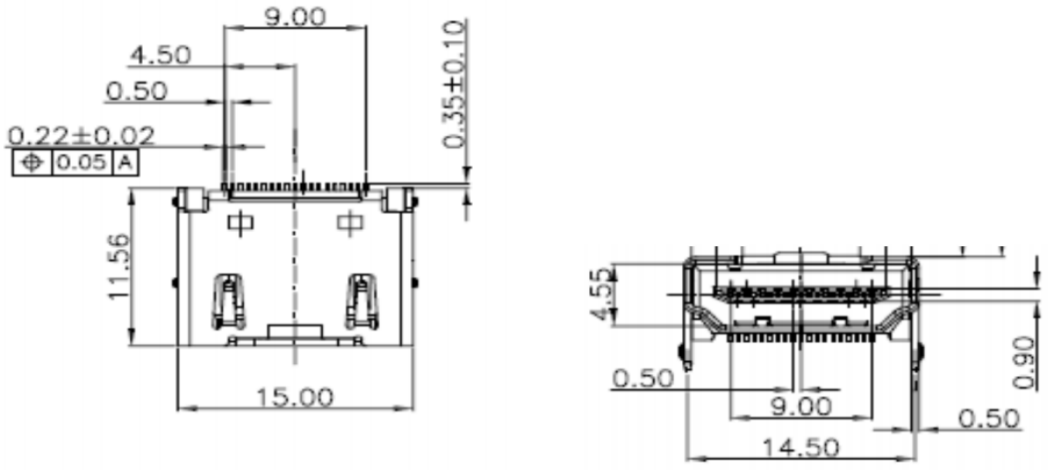


孔位 poles	A	B	C
2	2.00	8.00	4.75
3	4.00	10.00	6.75
4	6.00	12.00	8.75
5	8.00	14.00	10.75
6	10.00	16.00	12.75
7	12.00	18.00	14.75
8	14.00	20.00	16.75
9	16.00	22.00	18.75

2.6 HDMI PIN Defintion & Signal Connector

NO.	SYMBOL	DISCRIPTION	I/O
1	RX_D2+	HDMI Receiver channel 2 positive analog input.	I
2	GND	Ground.	P
3	RX_D2-	HDMI Receiver channel 2 negative analog input.	I
4	RX_D1+	HDMI Receiver channel 1 positive analog input.	I
5	GND	Ground.	P
6	RX_D1-	HDMI Receiver channel 1 negative analog input.	I
7	RX_D0+	HDMI Receiver channel 0 positive analog input.	I
8	GND	Ground.	P
9	RX_D0-	HDMI Receiver channel 0 negative analog input.	I
10	RX_CLK+	HDMI Receiver clock positive analog input.	I
11	GND	Ground.	P
12	RX_CLK-	HDMI Receiver clock negative analog input.	I
13	NC	No connect	
14	NC	No connect	
15	HDMI_SCL	HDMI Receiver DDC data channel.	I/O
16	HDMI_SDA	HDMI Receiver DDC clock channel.	I
17	GND	Ground.	P
18	HDMI_5V	HDMI Supply voltage (5.0V).	P
19	HPD	HDMI Receiver hot plug detect output	O

Note : HDMI Connector Dimension:



3. Operating Instructions:

3.1This product supports the following operating systems: Windows 7/8/10, Raspberry Pi, Ubuntu, Andriod.
3.2 Connect the HDMI cable to Windows 7/8/10 or Raspberry Pi or Ubuntu or Andriod.
3.3 Connect the CTP to micro USB.
3.4 Connect the micro USB DC POWER.

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	720	900	--		(1)(2)
Response time	Rising	$T_{R+}T_F$		--	30	40	msec	(1)(3)
	Falling							
Color gamut		S(%)			70		%	(1)
Color Filter Chromacicity	White	W_X		0.2759	0.3159	0.3559		(1)(4)
		W_Y		0.2991	0.3391	0.3791		
	Red	R_X		0.6184	0.6384	0.6584		
		R_Y		0.3166	0.3366	0.3566		
	Green	G_X		0.2905	0.3105	0.3305		
		G_Y		0.5788	0.5988	0.6188		
	Blue	B_X		0.1230	0.1430	0.1630		
		B_Y		0.0351	0.0551	0.0751		
Viewing angle	Hor.	$Θ_L$	CR>10	--	80	--		(1)(4)
		$Θ_R$		--	80	--		
	Ver.	$Θ_U$		--	80	--		
		$Θ_D$		--	80	--		
Option View Direction		ALL						(5)

4.2 Measuring Condition

■ Measuring surrounding：dark room

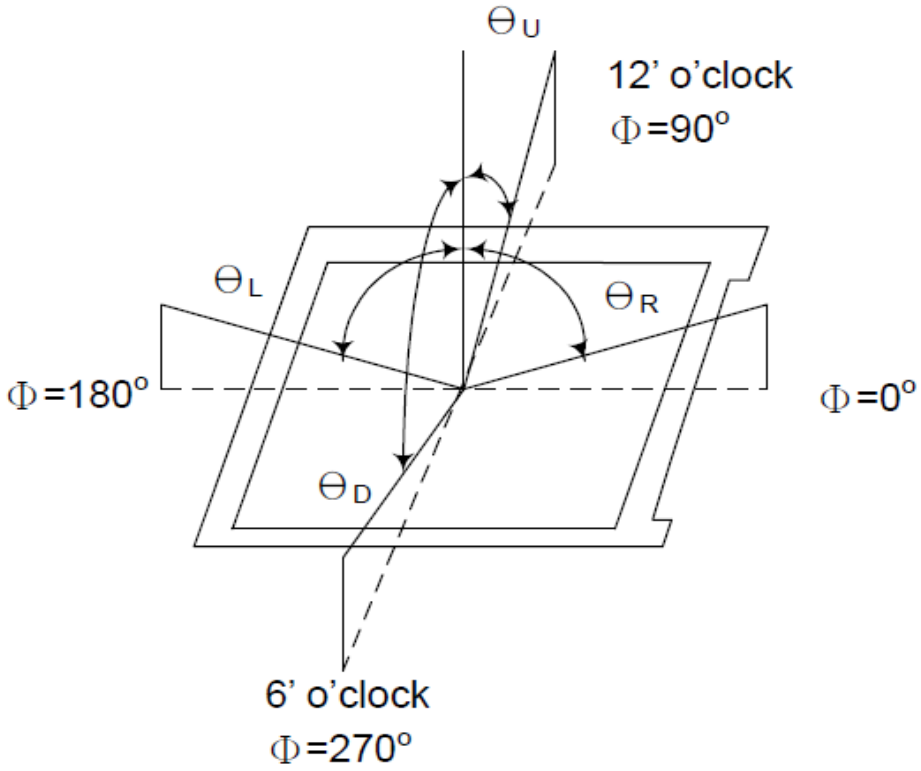
■ Ambient temperature：25±2oC

■ 15min. warm-up time.

4.3 Measuring Equipment

■ FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

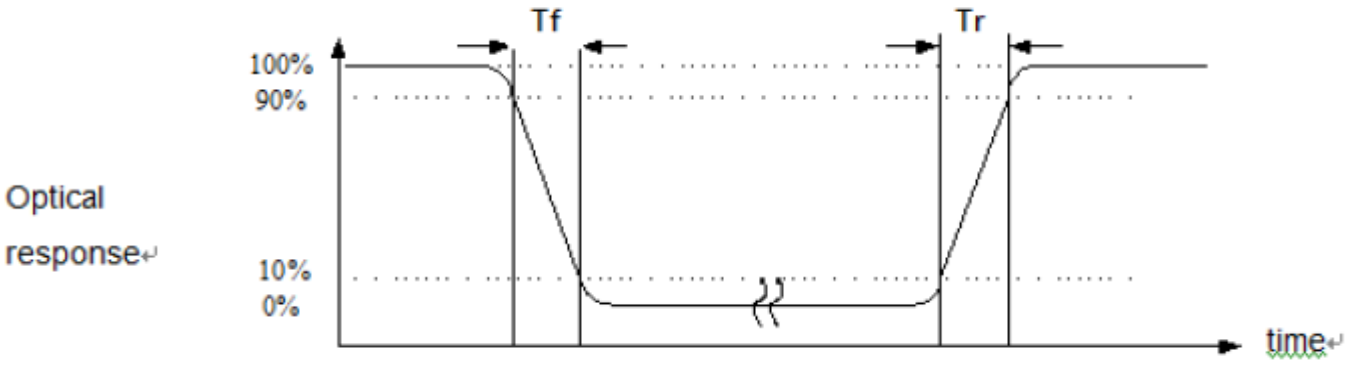
Note (1) Definition of Viewing Angle:



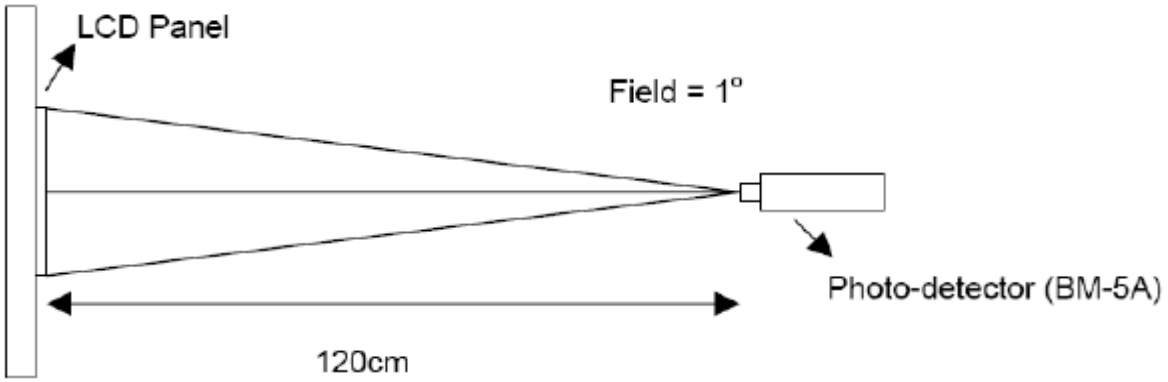
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

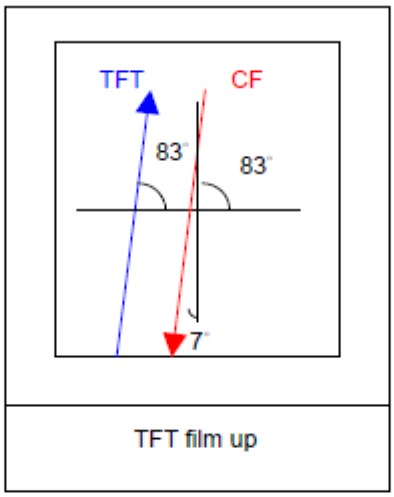
Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



5. Electrical Characteristics:

5.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Remake
Power supply voltage (Analog)	VDD-GND	-0.3	6.0	V	
	VDDp.GND	-0.3	6.0	V	
Input signal voltage (LED)	$V_{(LED)}$	-0.3	6.0	V	LED_EN
Input signal voltage (PWR)	$V_{(PWR)}$	-0.3	5.5	V	DCDC EN
Operating temperature	T_{OP}	-20	+70	℃	
Storage temperature	T_{ST}	-30	+80	℃	

NOTE1: If the products are exceeding the above range, they may be permanently damaged.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	--
Supply Voltage (Logic)	IOVCC	1.65	1.8	3.6	V	--
Normal mode Current consumption	IDD	--	TBD	--	mA	--
Level input voltage	V_{IH}	$0.7I_{OVCC}$	--	I_{OVCC}	V	--
	V_{IL}	GND	--	$0.3\ I_{OVCC}$	V	--
Level output voltage	V_{OH}	$0.8I_{OVCC}$	--	I_{OVCC}	V	--
	V_{OL}	GND	--	$0.2I_{OVCC}$	V	--

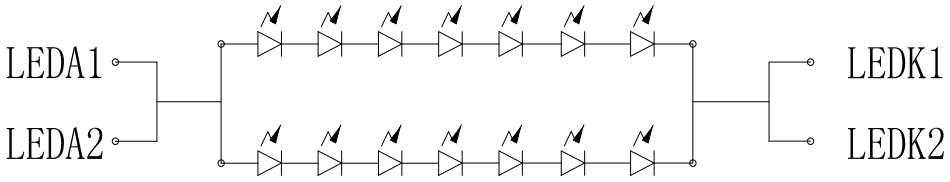
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 14 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	30	40	--	mA	--
Forward Voltage	V_F	--	22.4	--	V	--
LCM Luminance	L_V	310	360	--	cd/m2	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

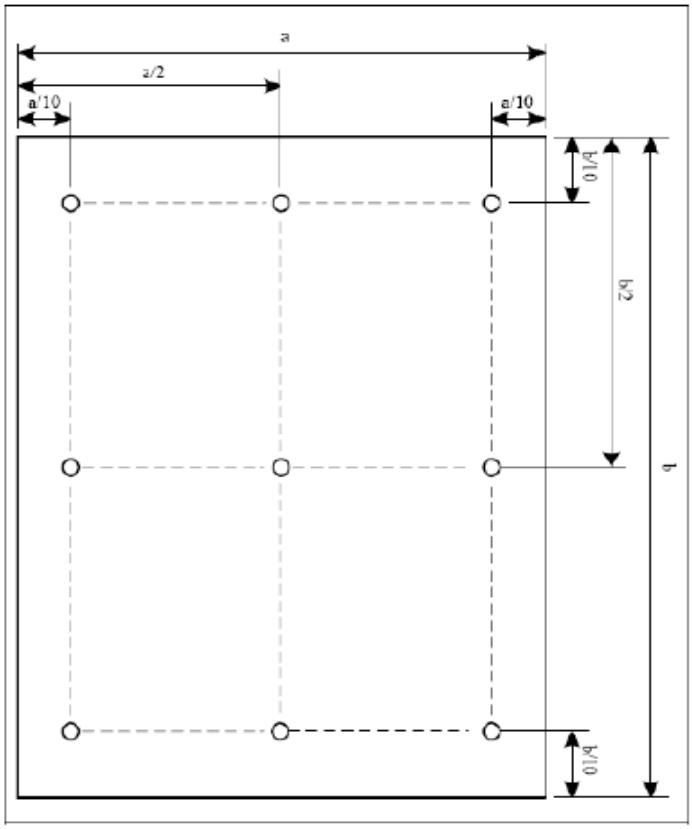
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



B1 CIRCUIT DIAGRAM

NOTE 3：Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. TFT AC Characteristic

6.1 High Speed Mode – Clock Channel Timing

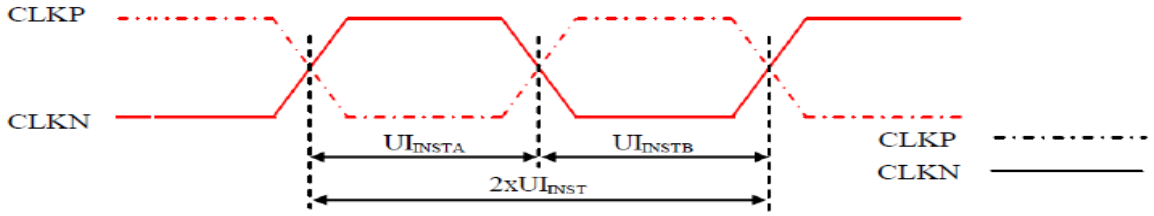


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

6.2 High Speed Mode – Data Clock Channel Timing

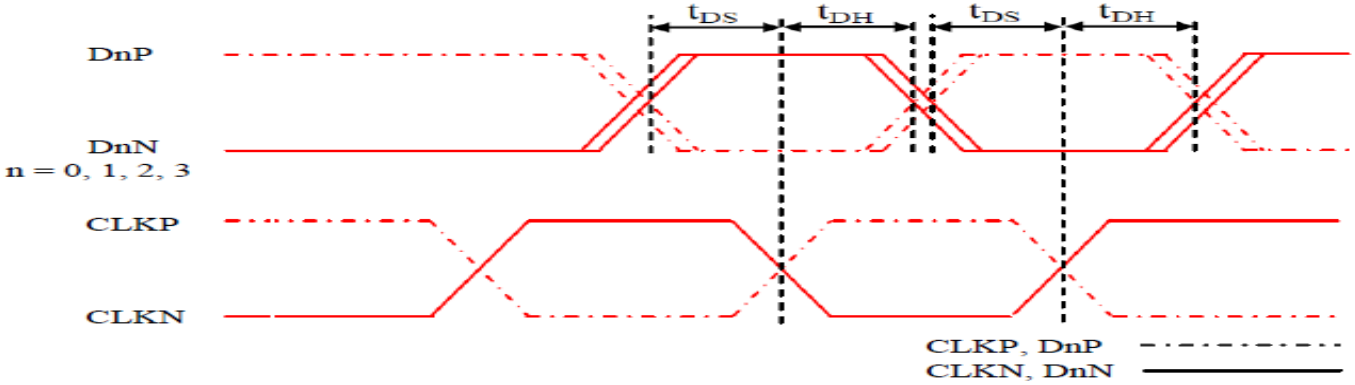


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6.3 High Speed Mode – Rise and Fall Timings

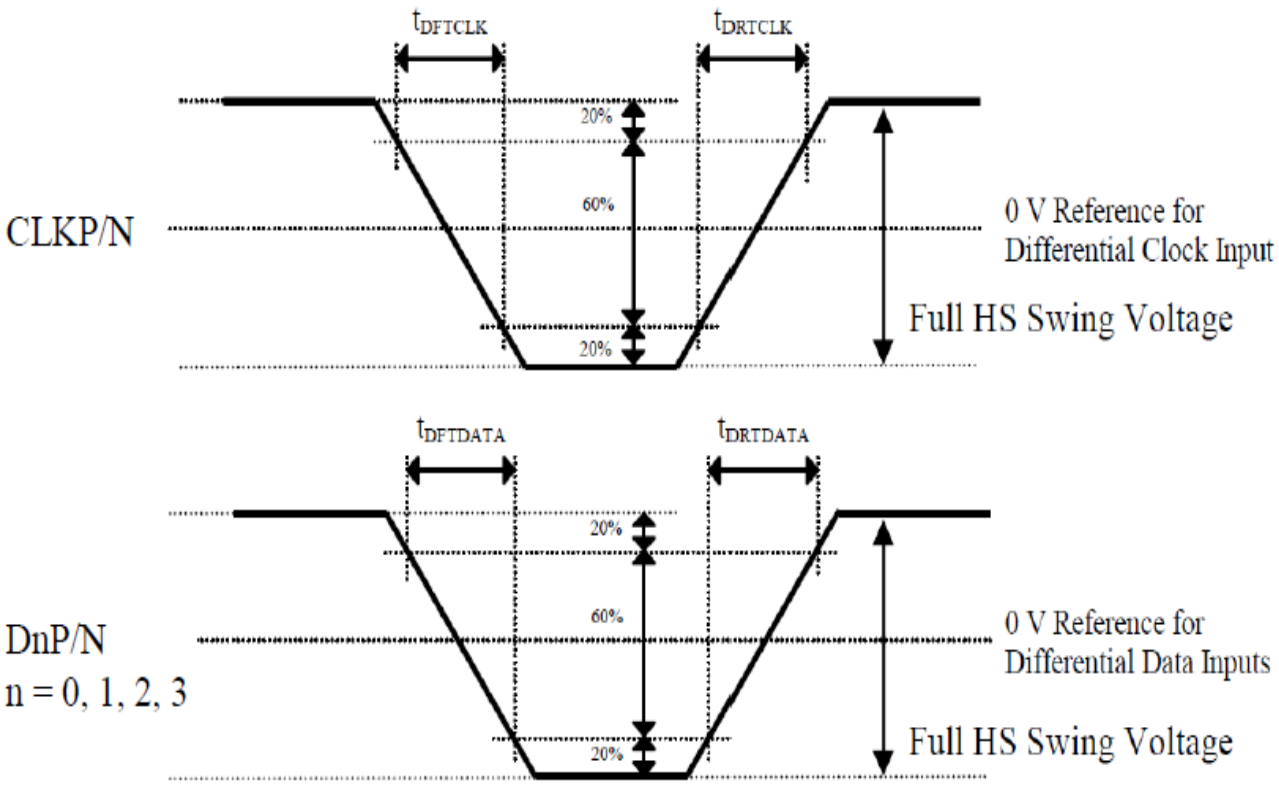


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

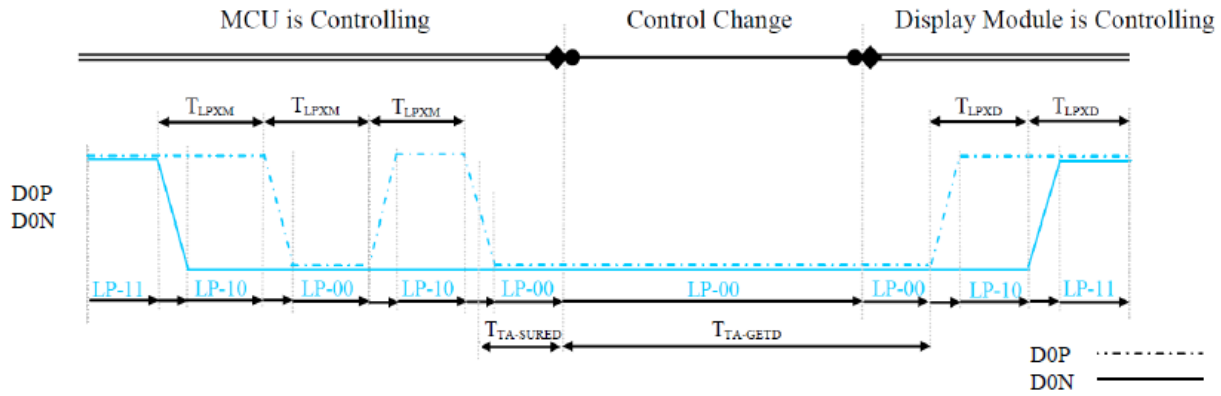
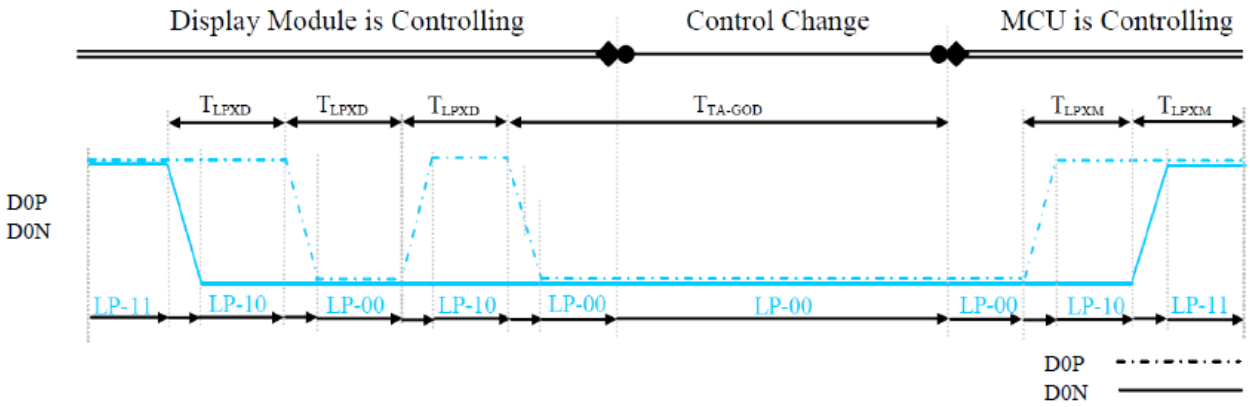


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

6.5 Data Lanes from Low Power Mode to High Speed Mode

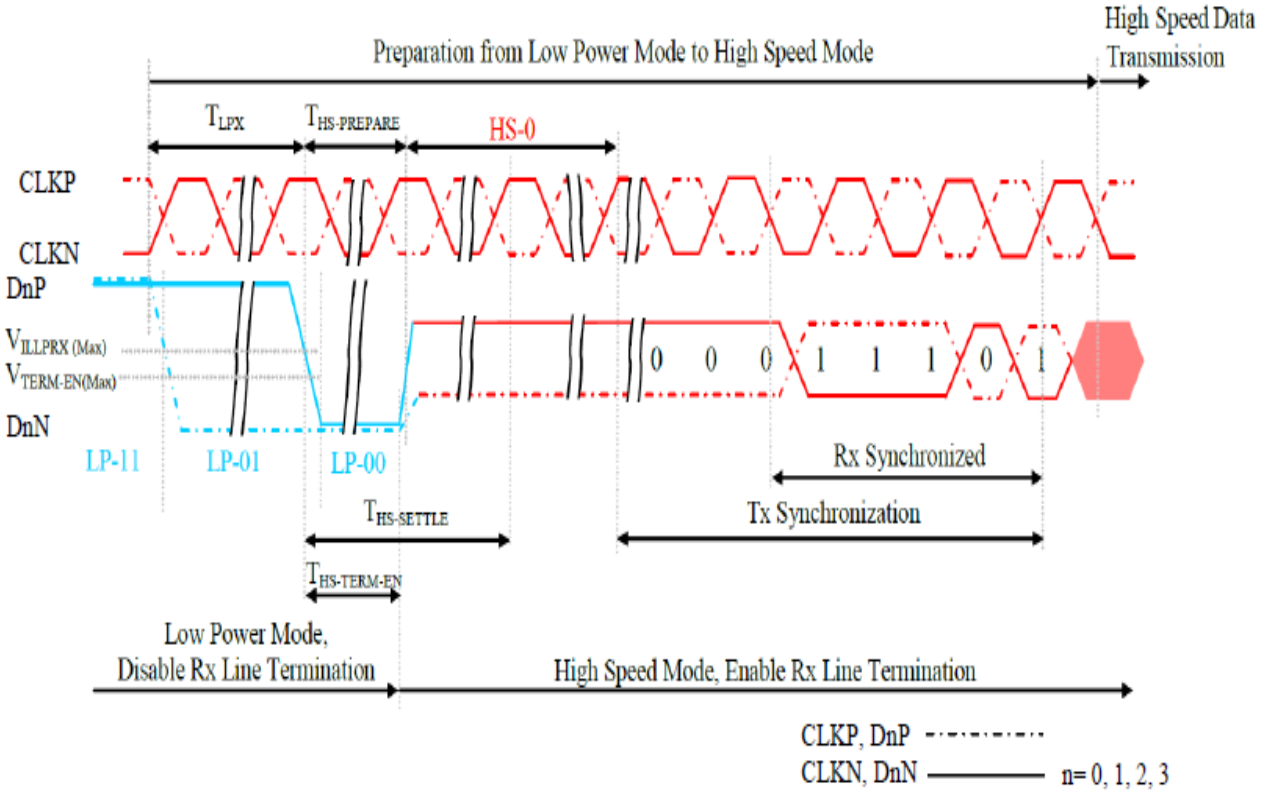
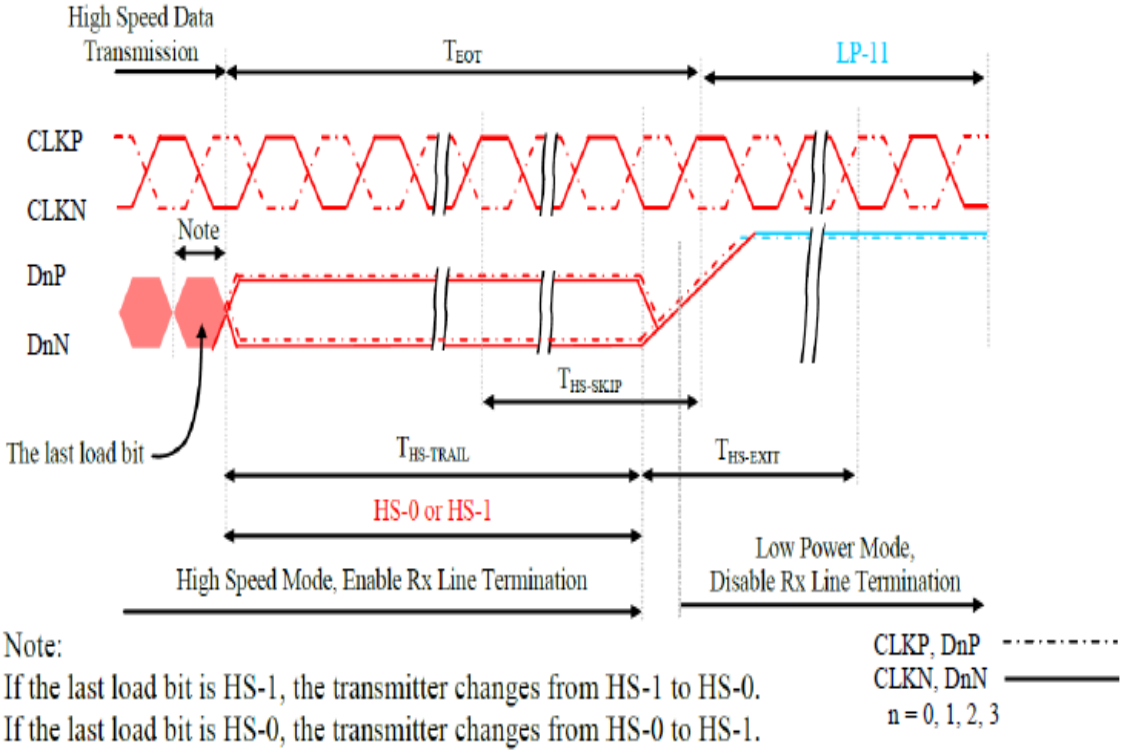


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

6.6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

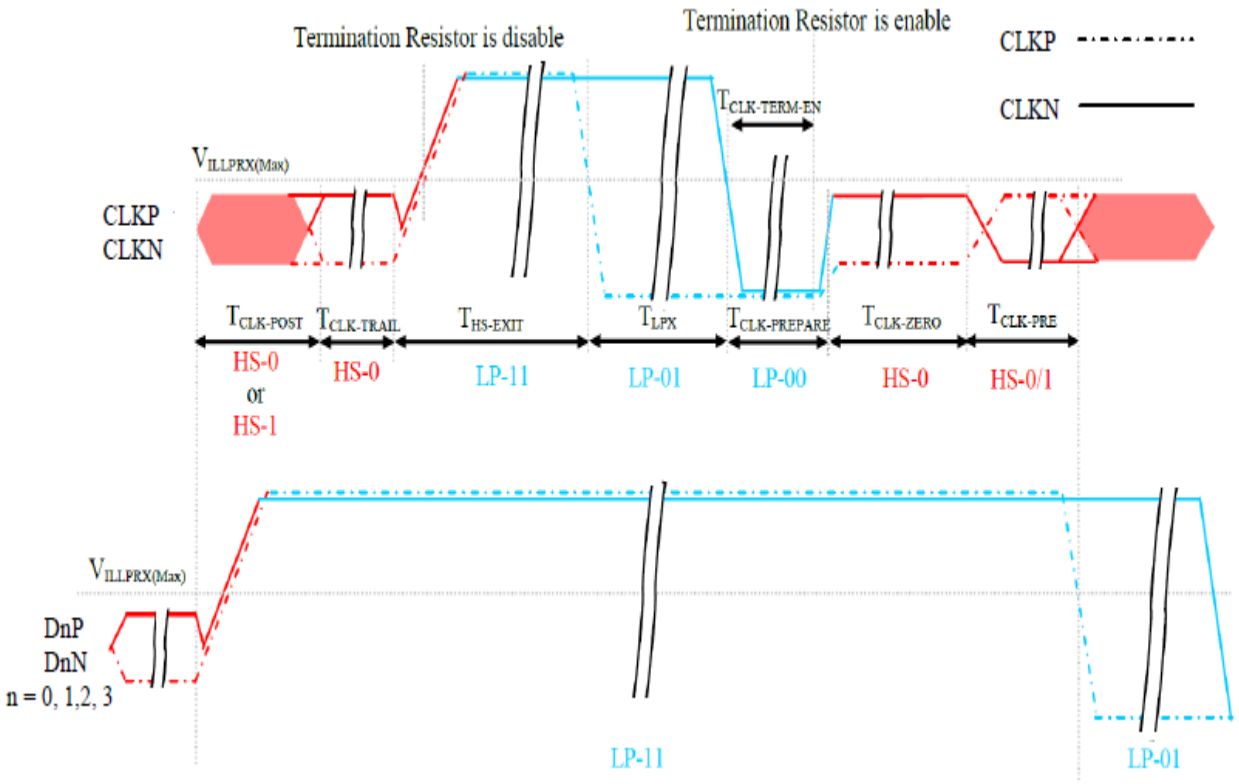
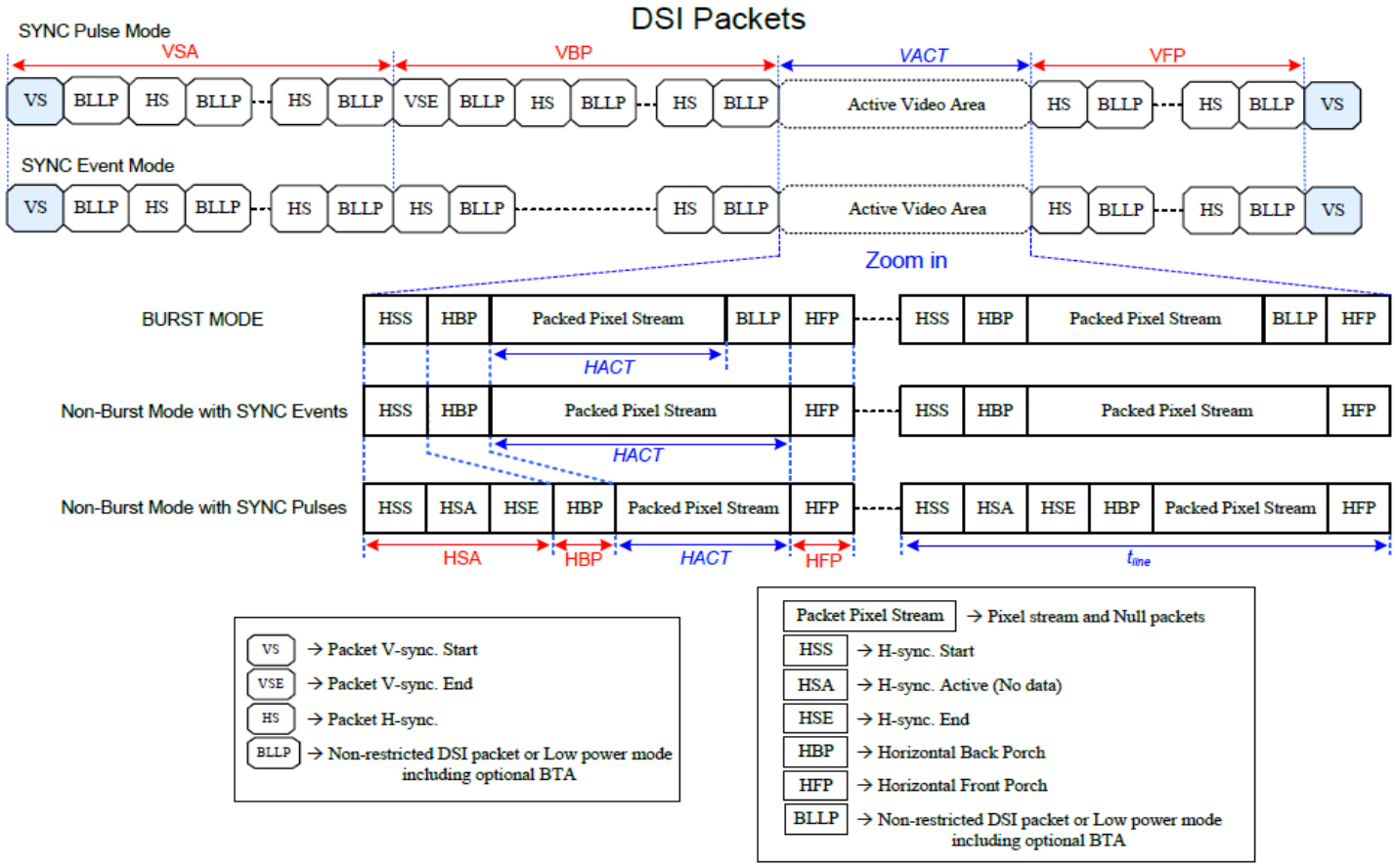


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

6.8 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.1DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to "Table 39: Limited Clock Channel Speed"

6.9 Reset input timing

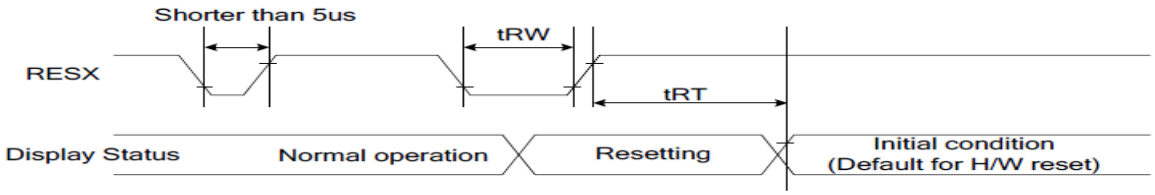


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

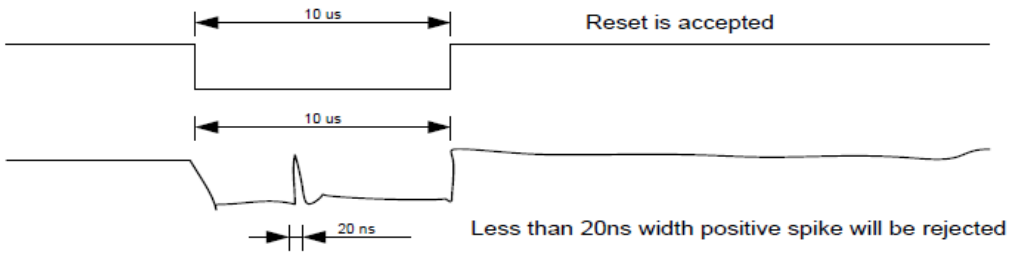


Figure 127: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	--
Operating temperature	T_{OP}	-20	+70	℃	--
Storage temperature	T_{ST}	-30	+80	℃	--

7.1.2 DC Electrical Characteristics (Ta=25℃)

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Min.	Typ.	Max.	Unit	Note
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDD	V	
Digital Input high voltage/VIH	0.75*VDD	--	VDD+0.3	V	
Digital Output low voltage/VOL	--		0.15*VDD	V	
Digital Output high voltage/VOH	0.85*VDD			V	

7.1.3 AC Characteristics

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC oscillation frequency	59	60	61	MHZ
I/O output rise time,low to high	-	14	-	ns
I/O output rfall time,high to low	-	14	-	ns

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

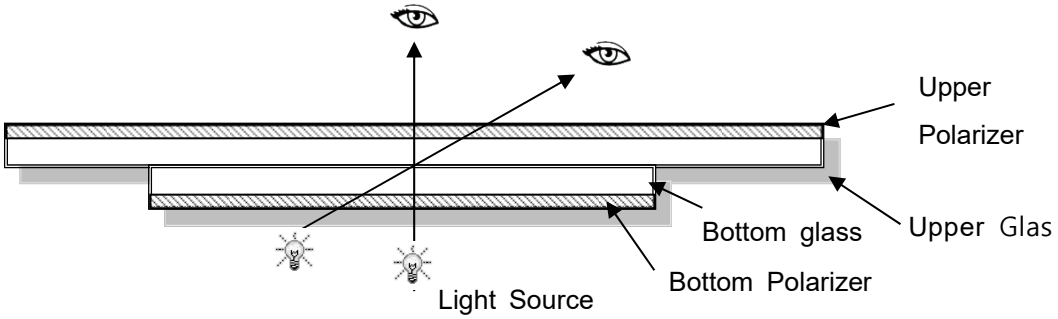
Temperature : 25±5℃

Humidity : 65%±10%RH

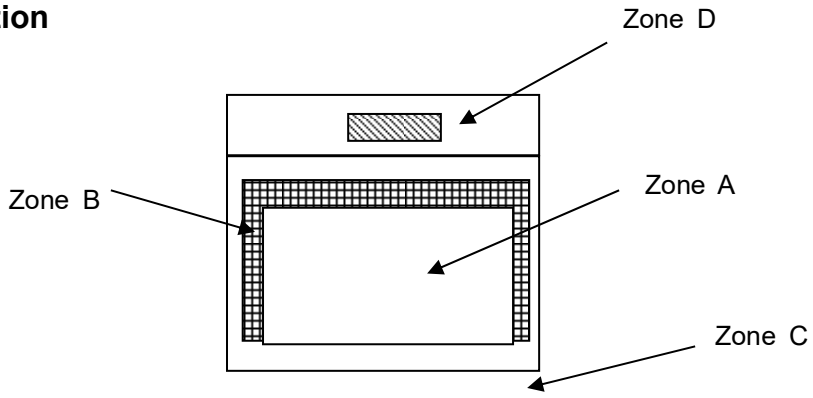
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C Cover (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

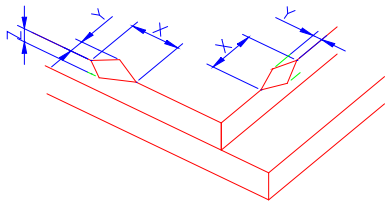
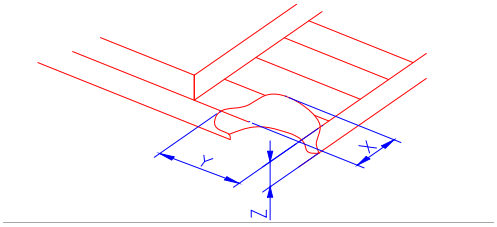
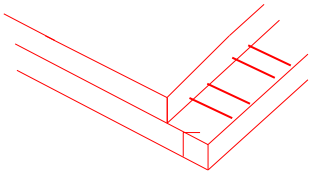
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

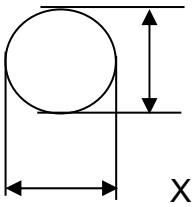
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.25	4(distance≧10mm)		
0.25<Φ≤0.35	3		
Φ>0.4	0		

②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.25	4(distance≧10mm)		
0.25<Φ≤0.35	3		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	3(distance≧10mm)		
Φ>0.5	1		

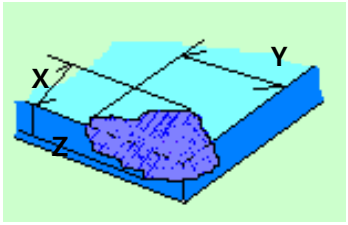
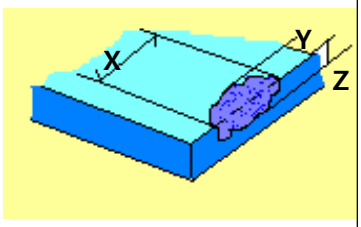
④Pixel bad points (light dot，Dim dot, color dot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore		Ignore
0.2<Φ≤0.3	2(distance≧10mm)		
Φ>0.4	1		

⑤ Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.4	4(distance≧10		
0.4<Φ≤0.5	3		
Φ>0.5	1		

<table>
<tr><td>3.0</td><td>Line defect (LCD/ TP /Polarizer backlight black/white line, scratch, stain)</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>Electronic Components SMT</td><td>Not allow missing parts，solderless connection，cold solder joint，mis match，The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color& Brightness</td><td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
<tr><td rowspan="2">6.0</td><td rowspan="2">CTP Related</td><td>CTP Cover sensor accidented black/white spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.25</td><td colspan="2">4（distance≧10mm）</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">3</td></tr>
<tr><td>Φ>0.4</td><td colspan="2">1</td><td></td></tr>
</table>
</td></tr>
<tr><td>CTP Cover scratch</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Ignore (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="3">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
</table>

		CTP Cover Pinhole/ Lack of ink	<table><tr><td>Zone / Size (mm)</td><td>Acceptable Qty</td></tr><tr><td></td><td>C</td></tr><tr><td>Φ≤0.2</td><td>Ignore</td></tr><tr><td>0.2<Φ≤0.3</td><td>4(distance≧10mm)</td></tr><tr><td>0.3<Φ≤0.4</td><td>3</td></tr><tr><td>Φ>0.4</td><td>0</td></tr></table>
		CTP Bonding bubble/ accidented spot	<table><tr><td rowspan="2">Size Φ(mm)</td><td colspan="2">Acceptable Qty</td></tr><tr><td>A</td><td>B</td></tr><tr><td>Φ≤0.1</td><td colspan="2">Ignore</td></tr><tr><td>0.15<Φ≤0.2</td><td colspan="2">2(distance＞10mm)</td></tr><tr><td>0.2<Φ≤0.25</td><td colspan="2">2</td></tr><tr><td>Φ>0.25</td><td colspan="2">0</td></tr></table>
		Assembly deflection	beyond the edge of backlight ≤0.2mm
		TP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤0.5mm</td><td>Y≤0.5mm</td><td>Z<cover thickness</td></tr></table> * Circuitry broken is not allowed. 
		TP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤0.3mm</td><td>Y≤0.3mm</td><td>Z<LCD thickness</td></tr></table> * Circuitry broken is not allowed. 

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90％RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	- 30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing

----TBD----------