



SPECIFICATION FOR LCM+CTP Module

MODULE No:	KD070HDFIA018-01-C028A
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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1.Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, capacitance touch panel back-light unit. The resolution of a 7.0 " TFT-LCD contains 1024x600 pixels, and can display up to 16.7M colors.

1.1 TFT Features

General Information	Items	Specification	Unit	Note
		Main Panel		
	Display area(AA)	154.21(H)*85.92 (V) (7.0inch)	mm	
	Driver element	TFT active matrix	-	
	Display colors	16.7M	colors	
	Number of pixels	1024(RGB)*600	dots	
	Pixel arrangement	RGB vertical stripe	-	
	Pixel pitch	0.1506(H)*0.1432(V)	mm	
	Viewing angle	Free	o'clock	
	Controller IC	EK73217BCGA+EK79007AD	-	
	LCM Interface	4Lane MIPI	-	
	Display mode	Transmissive /Normally Black	-	
	Touch and LCM Bonding technology	Tape bonding	-	
	Operating temperature	-20~+70	℃	
	Storage temperature	-30~+80	℃	

1.2 CTP Features

General Information	Items	Specification	Unit	Note
		Main Panel		
	Resolution	1024(H)*600(V)	-	
	Structure	G+G	-	
	Controller IC	GT9271	-	
	Interface	I2C	-	
	Slave Address	0x5D(7bit) or 0x14(7bit)	-	Note1
	Touch mode	Ten points and Gestures	-	-

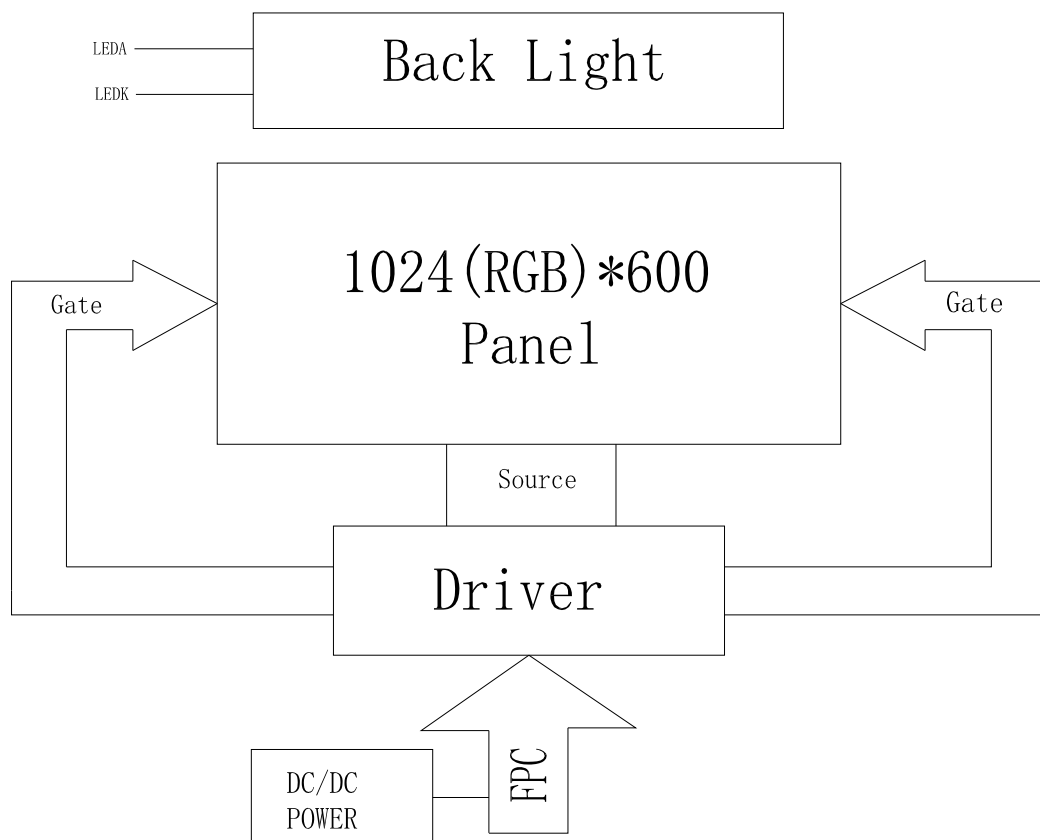
Note1: For specific configuration method, please refer to section 8.2

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1.3 Mechanical Information

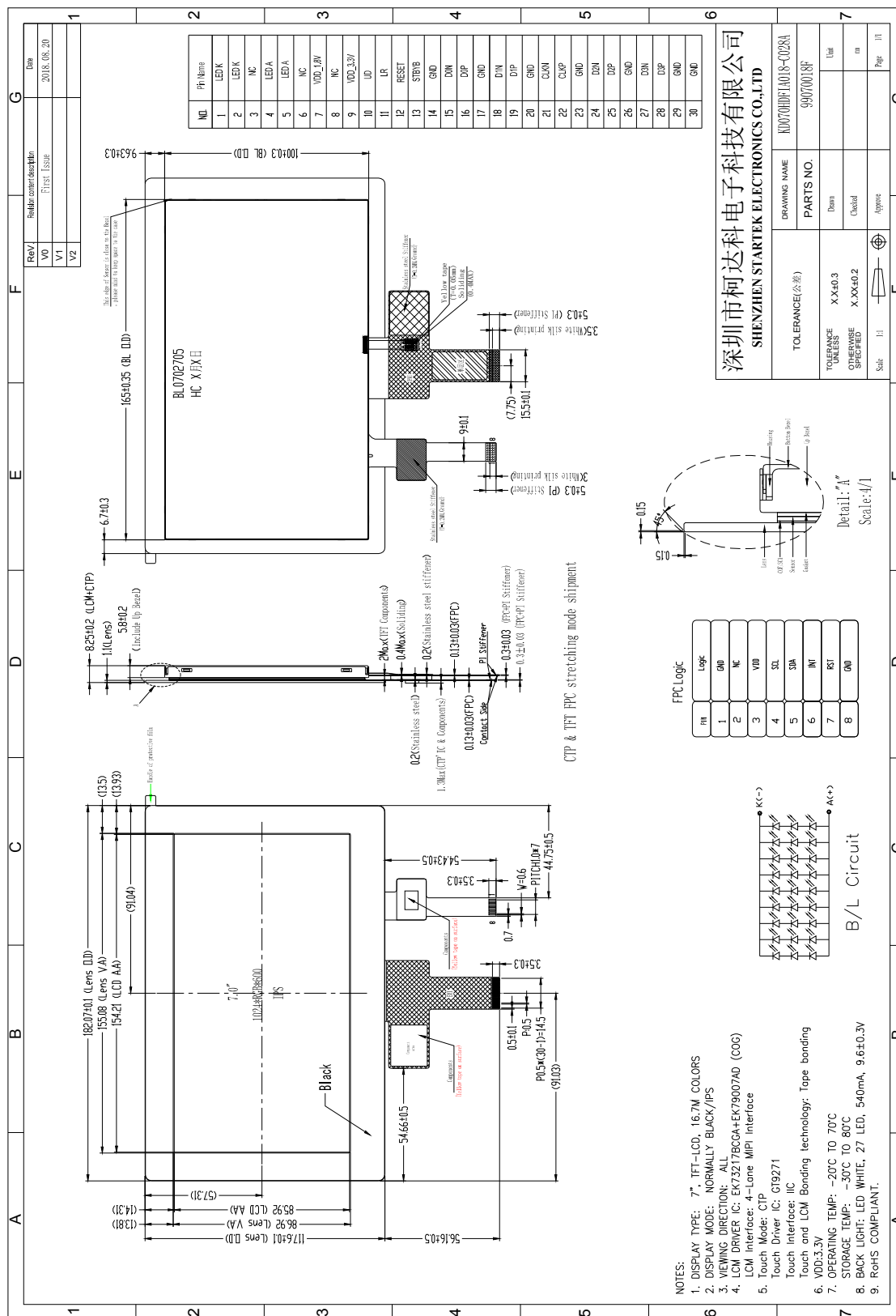
Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	182.07	-	mm	
	Vertical(V)	-	117.60	-	mm	
	Depth(D)	-	8.25	-	mm	
Weight		-	--	-	g	

2. Block Diagram



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3. Outline dimension



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4. Input terminal Pin Assignment

4.1 TFT PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	LEDK	LED Cathode	P
2	LEDK	LED Cathode	P
3	NC		
4	LEDA	LED Anode	P
5	LEDA	LED Anode	P
6	NC		
7	VDD_1.8V	Power supply for digital circuits	P
8	NC		
9	VDD_3.3V	Power supply for DC/DC convert circuit	P
10	UD	Vertical shift direction (gate output) selection(NOTE1)	I
11	LR	Horizontal shift direction (source output) selection(NOTE1)	I
12	RESET	Global reset pin. Active low to enter reset state.	I
13	STBYB	Standby mode, Normally pulled high STBYB = "1", normal operation STBYB = "0", timing controller, source driver will turn off, all o utput are High-Z.	I
14	GND	Ground	P
15	D0N	MIPI DSI differential data pair (Data lane 0)	I/O
16	D0P		
17	GND	Ground	P
18	D1N	MIPI DSI differential data pair (Data lane 1)	I/O
19	D1P		
20	GND	Ground	P
21	CLKN	MIPI DSI differential clock pair .	I
22	CLKP		
23	GND	Ground	P
24	D2N	MIPI DSI differential data pair (Data lane 2)	I/O
25	D2P		

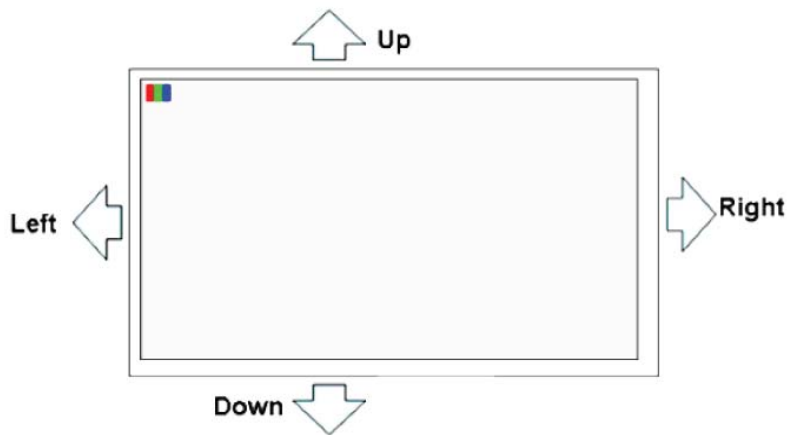
26	GND	Ground	P
27	D3N	MIPI DSI differential data pair (Data lane 3)	I/O
28	D3P		
29	GND	Ground	P
30	GND	Ground	P

Note1: When L/R="0", set right to left scan direction.

When L/R="1", set left to right scan direction.

When U/D="0", set top to bottom scan direction.

When U/D="1", set bottom to top scan direction.



4.2 CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	NC	No Connection	
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

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5. LCD Optical Characteristics

5.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	600	800	--		Note 2
Response time	Rising	T _R +T _F		--	25	40	msec	Note 5
	Falling							
Uniformity		S(%)		--	50	--	%	Note 3
Color Filter Chromaticity	White	W _X	Θ = 0°	0.270	0.310	0.350		Note 4 C light
		W _Y		0.300	0.340	0.380		
	Red	R _X		0.568	0.608	0.648		
		R _Y		0.316	0.356	0.396		
	Green	G _X		0.271	0.311	0.351		
		G _Y		0.541	0.581	0.621		
	Blue	B _X		0.111	0.151	0.191		
		B _Y		0.068	0.108	0.148		
Viewing angle	Hor.	Θ _L	CR>10	--	85	--		Note 1
		Θ _R		--	85	--		
	Ver.	Θ _U		--	85	--		
		Θ _D		--	85	--		
Option View Direction		FREE						

- Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer
4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_d .

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6. Electrical Characteristics

6.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Power supply for digital circuits	VDD_1.8V	-0.3	2.0	V	Note1
Power supply for DC/DC convert circuit	VDD_3.3V	-0.3	6.0	V	Note1
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply for digital circuits	VDD_1.8V	1.71	1.8	1.89	V	
Power supply for DC/DC convert circuit	VDD_3.3V	2.7	3.3	5.8	V	
Normal mode Current	IDD_1.8V	--	0.05	--	mA	
Normal mode Current	IDD_3.3V	--	200	--	mA	
Low Level input voltage	V _{IH}	0.7*VDD_1.8V	--	VDD_1.8V	V	
	V _{IL}	0	--	0.3*VDD_1.8V	V	

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High Level output voltage	V _{OH}	VDD_1.8 V-0.4	--	VDD_1.8 V	V	
	V _{OL}	0	--	0.4	V	

6.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 27 chips LED

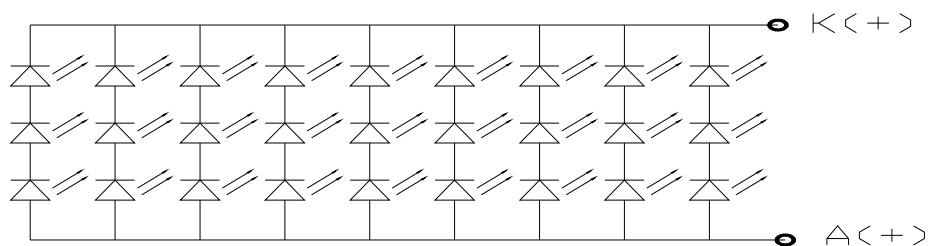
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	--	540	--	mA	
Forward Voltage	V _F	--	9.6	--	V	
LCM Luminance (I _F =180mA)	LV	1044	1144	--	cd/m2	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

T_a=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at

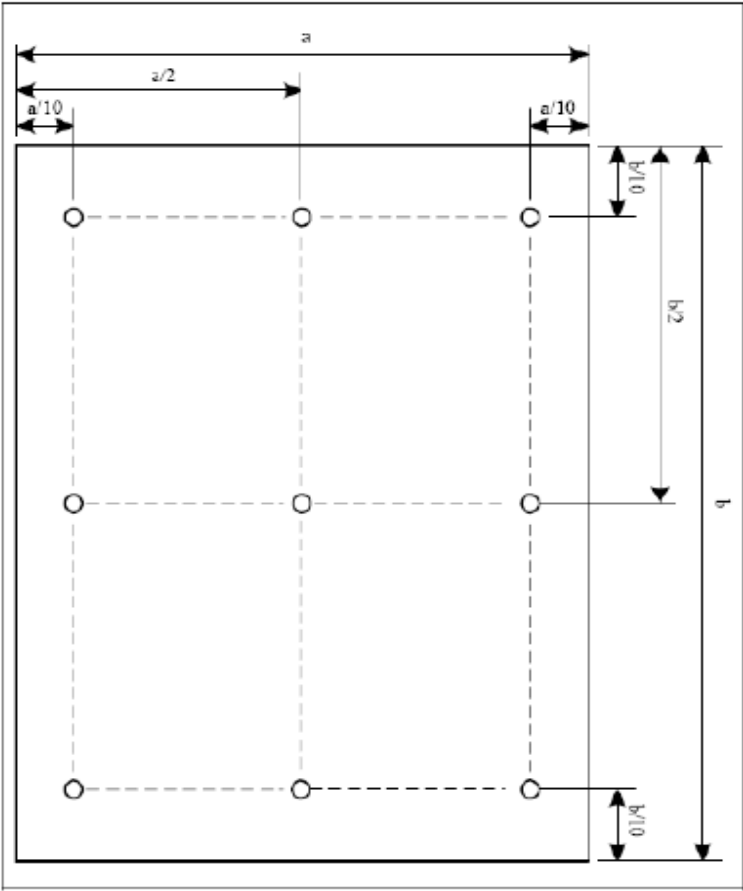
T_a=25°C and I_L=540mA. The LED lifetime could be decreased if operating I_L is larger than 540mA. The constant current driving method is suggested.



B/L Circuit

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Note (3) Luminance Uniformity of these 9 points is defined as below:



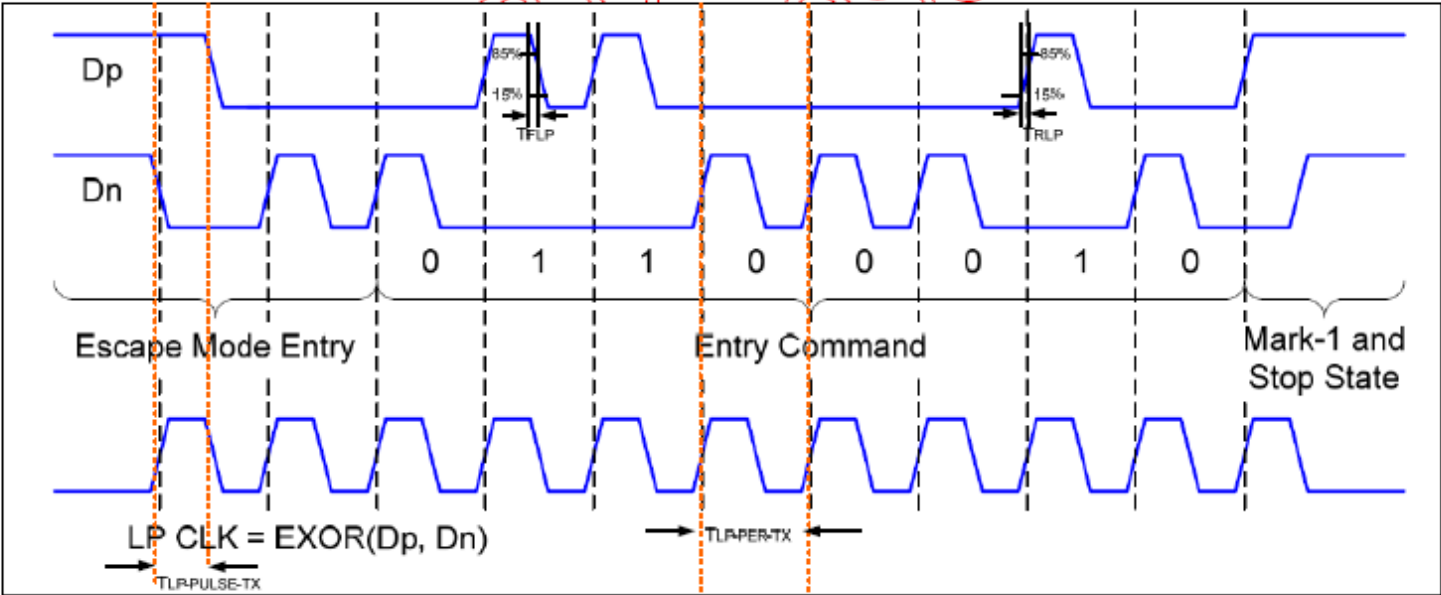
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. MIPI AC Characteristic

7.1 LP Transmitter AC Specification

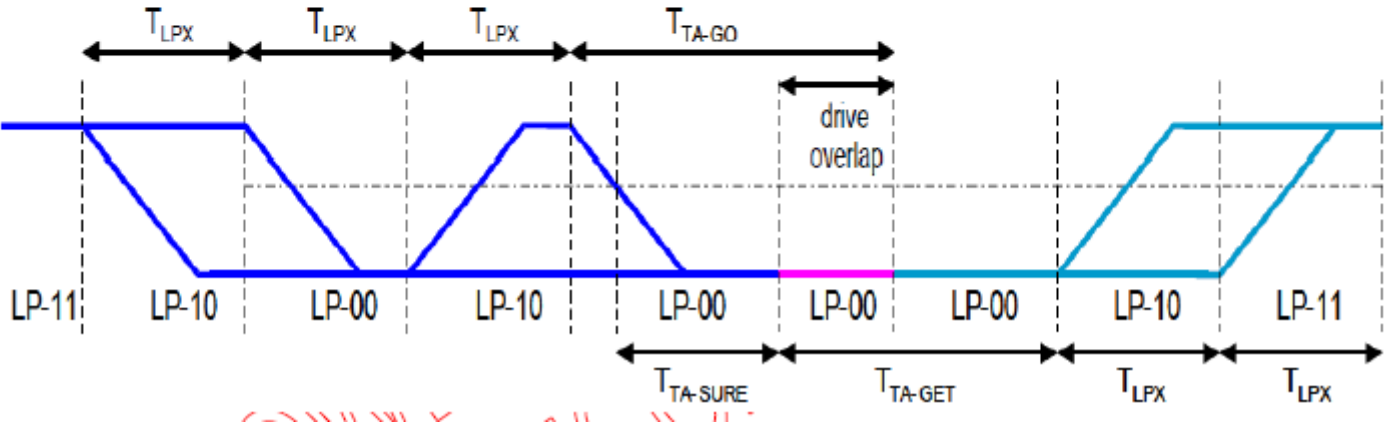
Parameter	Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time	T_{RLP} / T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time	T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	$T_{LP-PULSE-TX}$	40	-	-	ns	-
		20	-	-	ns	-
Period of the LP EXOR clock	$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @CLOAD =0pF	$\delta V / \delta t_{SR}$	30	-	500	mV/ns	-
Slew Rate @CLOAD =5pF		30	-	200	mV/ns	-
Slew Rate @CLOAD =20pF		30	-	150	mV/ns	-
Slew Rate @CLOAD =70pF		30	-	100	mV/ns	-
Load Capacitance	T_{RLP}	-	-	70	pF	-



7.2 Turnaround Procedure

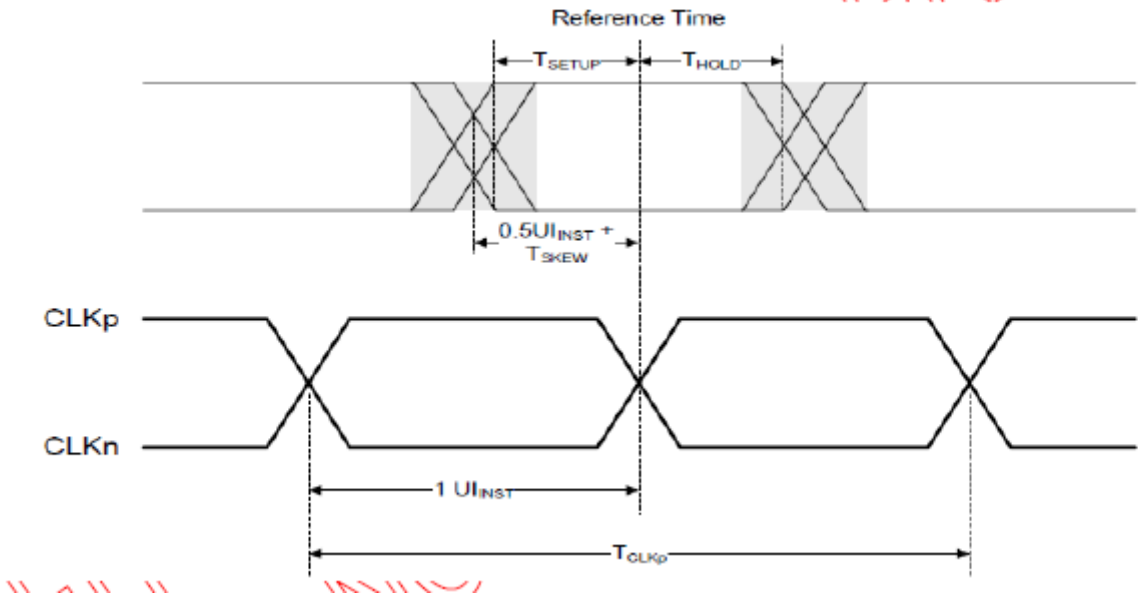
Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period: Master side	T _{LPX}	50	-	75	ns
Length of any Low-Power state period: Slave side	T _{LPX}	50	55.56	58.34	ns
Ratio of T _{LPX} (Master)/ T _{LPX} (Slave) between Master and Slave side	Ratio T _{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	T _{TA-Sure}	T _{LPX}	-	2T _{LPX}	ns
Time to drive LP-00 by new TX	T _{TA-GET}	-	5T _{LPX}	-	ns
Time to drive LP-00 after Turnaround Request	T _{TA-GO}	-	4T _{LPX}	-	ns



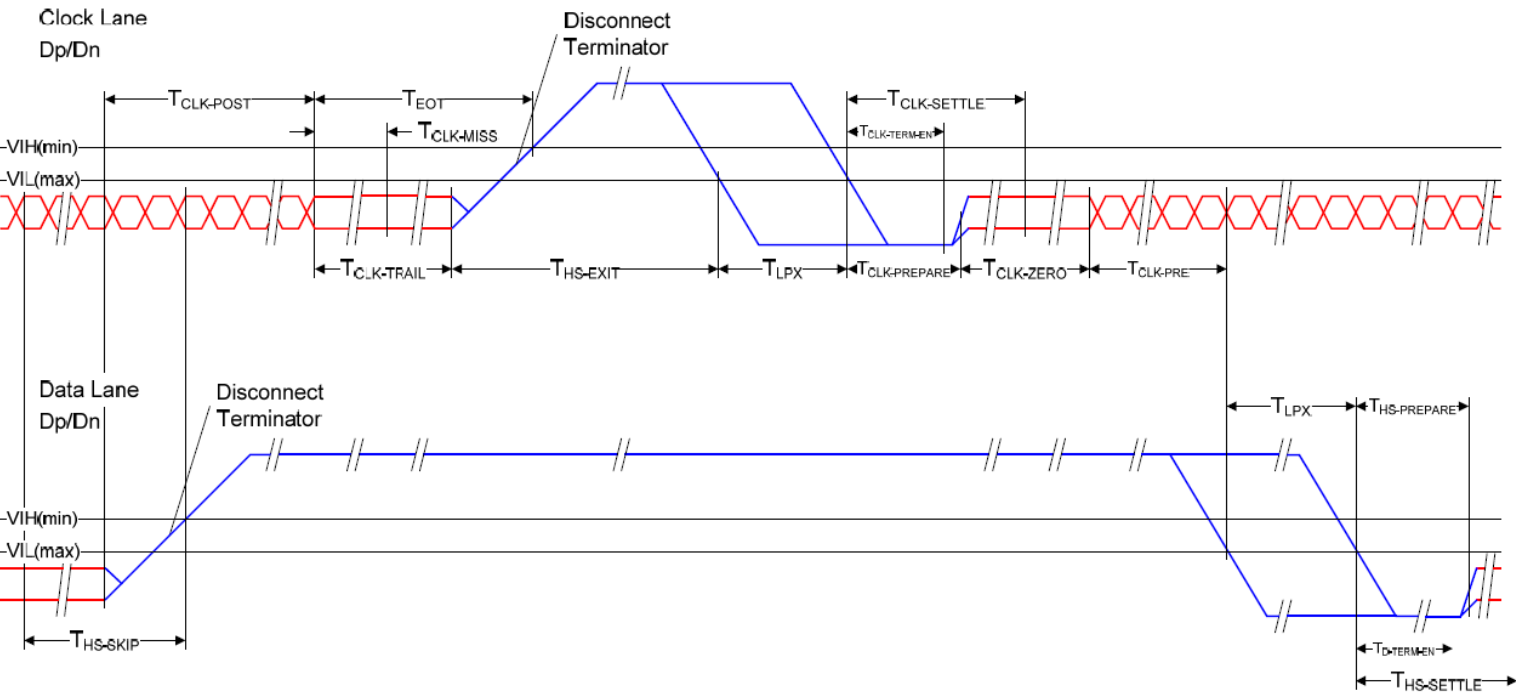
7.3 High speed transmission

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI _{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter)	T _{SKEW(TX)}	-0.15	-	0.15	UI _{INST}
Data to Clock Setup time(measured at receiver)	T _{SETUP(RX)}	0.15	-	-	UI _{INST}
Data to Clock Hold time(measured at receiver)	T _{HOLD(RX)}	0.15	-	-	UI _{INST}
20%~80% rise time and fall time	T _R , T _F	150	-	-	ps
		-	-	0.3	UI _{INST}



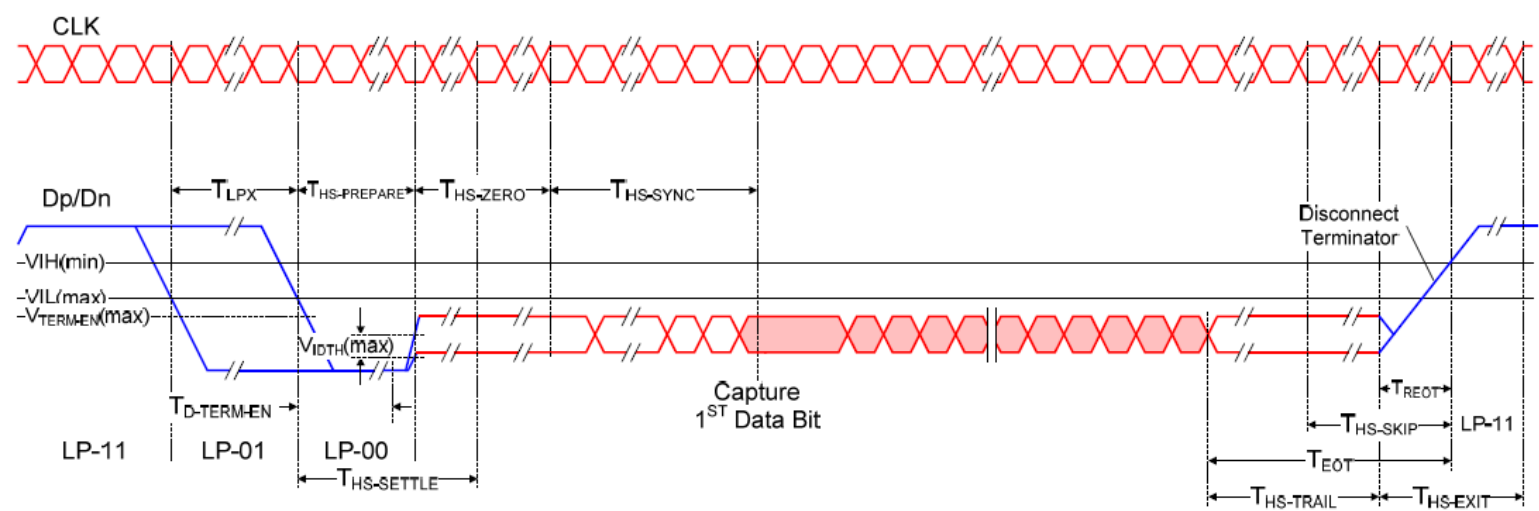
7.4 High Speed Clock Transmission

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	TCLK-MISS	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38	-	95	ns
Minimum lead HS-0 drive period before starting clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VILMAX	THS-TERM-EN	-	-	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	TCLK-PRE	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns





7.5 High Speed Data Transmission in Bursts



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8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

8.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VDD	2.66	3.3	3.47	V	
Normal mode operating current	--	13	--	mA	
Green mode operating current	--	4.5	--	mA	
Sleep mode operating current	70	--	120	uA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDD	V	
Digital Input high voltage/VIH	0.75*VDD	--	VDD+0.3	V	
Digital Output low voltage/VOL	--	--	0.15*VDD	V	
Digital Output high voltage/VOH	0.85*VDD	--	--	V	

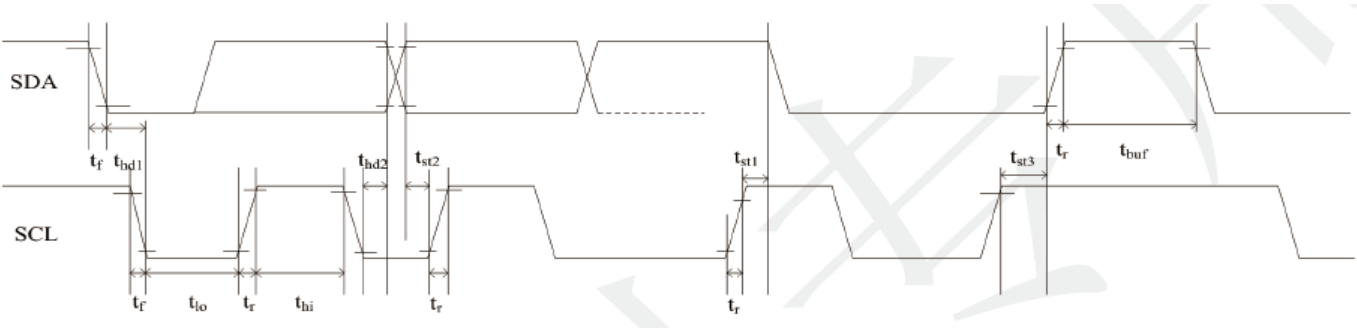
8.1.3 AC Characteristics

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit	Note
OSC oscillation frequency	59	60	61	MHZ	
I/O output rise time,low to high	-	14	-	ns	
I/O output rfall time,high to low	-	14	-	ns	

8.2 I2C Timing

GT9271 provides a standard I2C interface for SCL and SDA to communicate with the host. GT9271 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:





Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

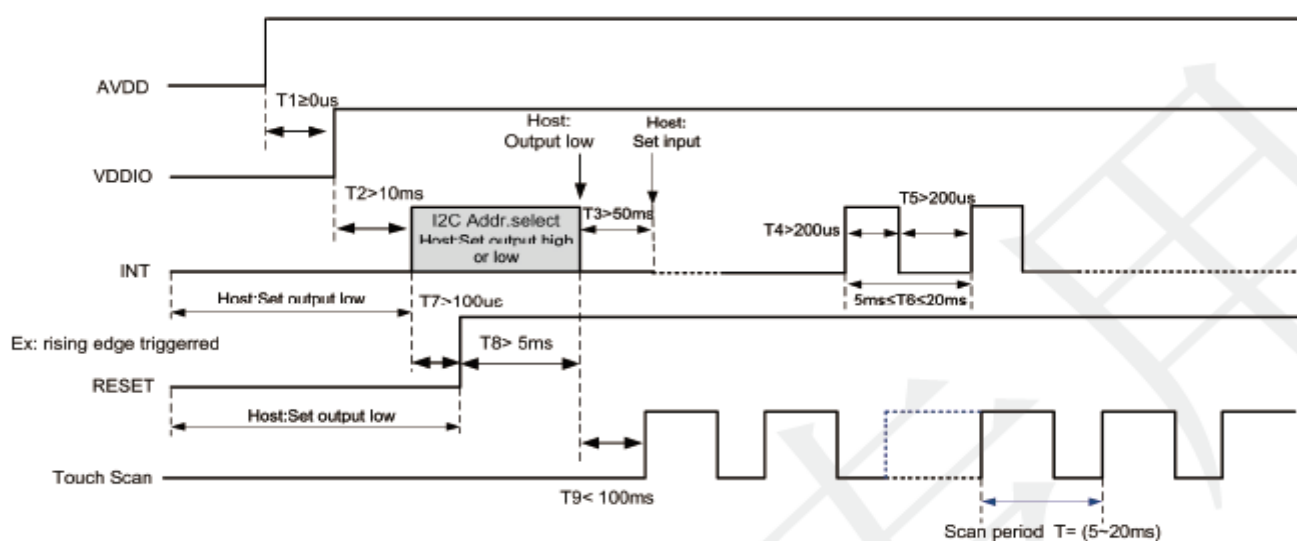
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

GT9271 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

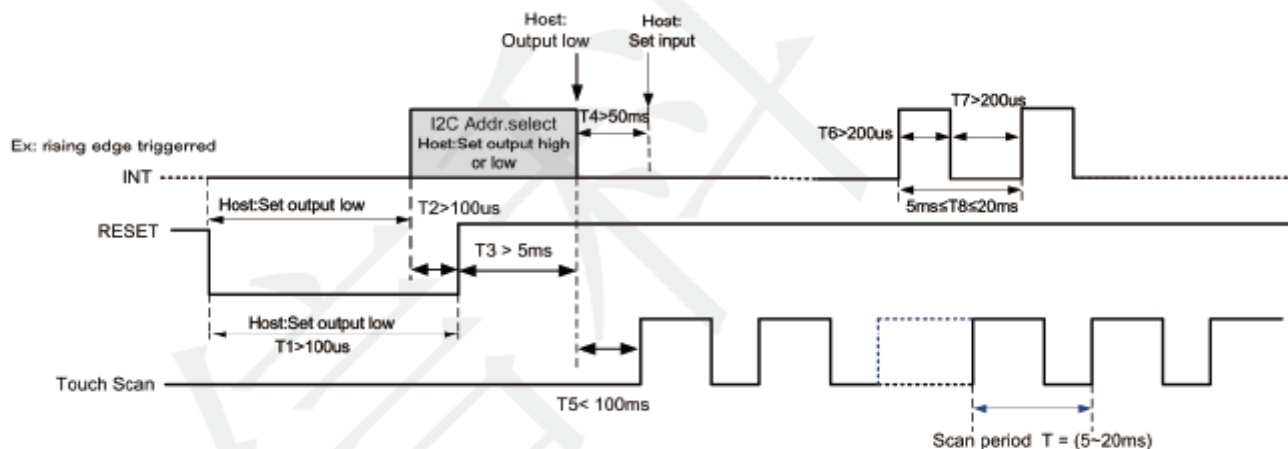
Power-on Timing:



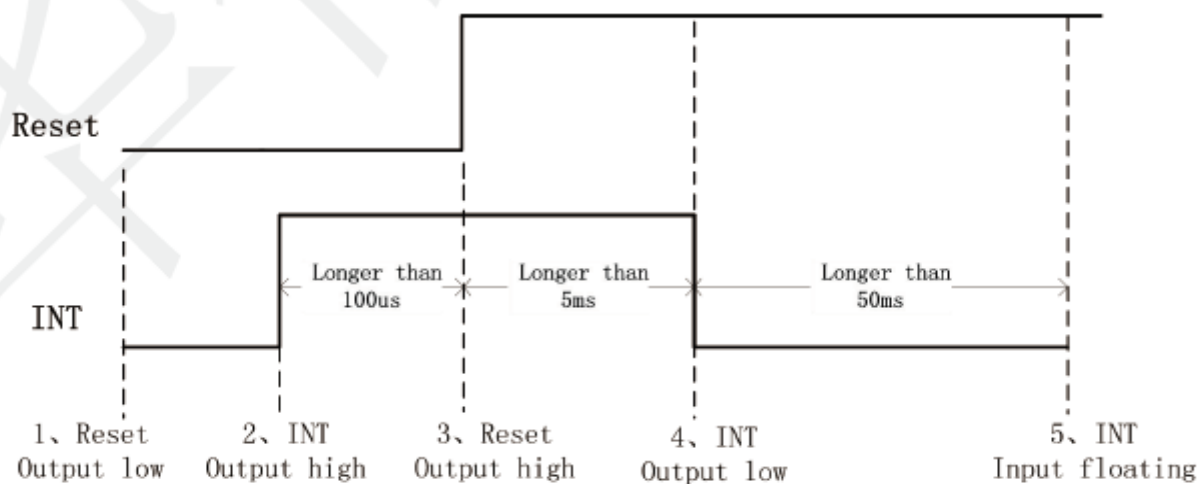
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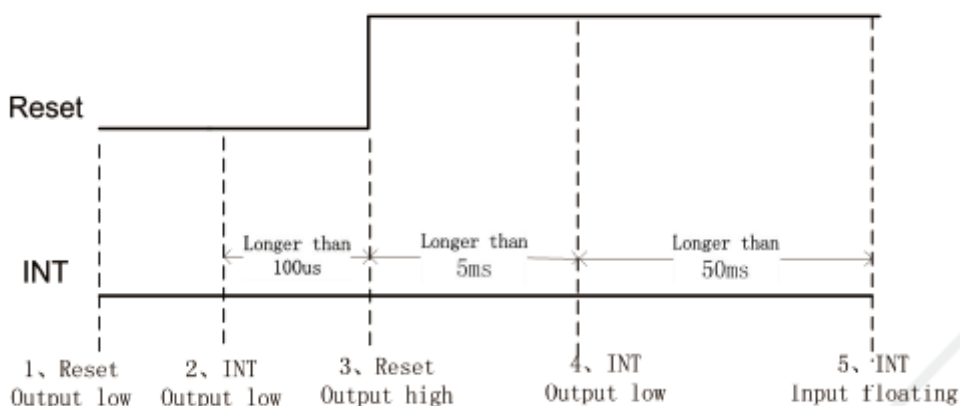
Timing for host resetting GT9271:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



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a) Data Transmission

(For example: slave address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from high to low when SCL line is high. Data flow or address is transmitted after the Start condition.

All slave devices connected to I²C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT9271 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0xBA or 0xBB, GT9271 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high.

When communication is completed, the host will issue the Stop condition which implies the transition of SDA line from low to high when SCL line is high.

b) Writing Data to GT9271

(For example: slave address is 0xBA/0xBB)



Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT9271. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

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c) Reading Data from GT9271

(For example: slave address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT9271. First, the host issues a Start condition and sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operation). After receiving ACK, the host starts to read data.

GT9271 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

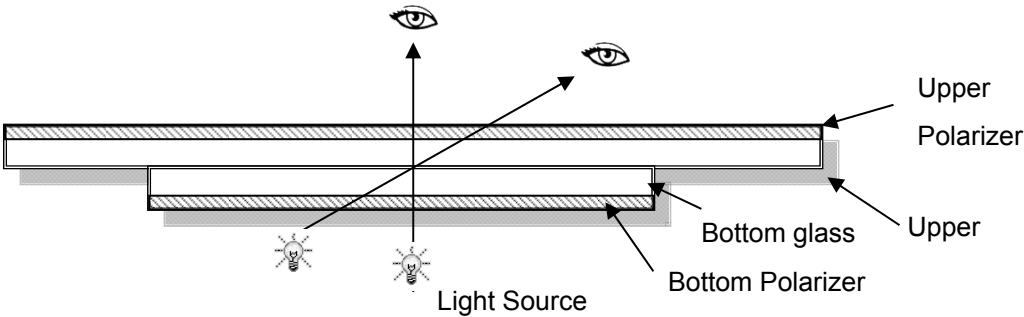
9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

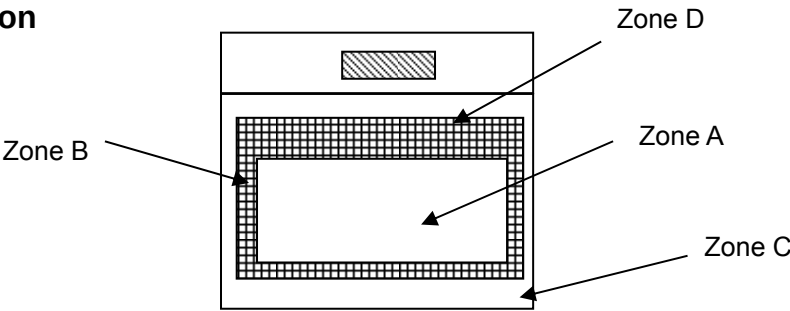
9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



9.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
 - Zone B : Viewing Area except Zone A
 - Zone C Cover (Zone A+Zone B) which can not be seen after assembly by customer .)
 - Zone D : IC Bonding Area
- Note:
- As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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9.1.3 Sampling Plan

According to GB/T 2828.1-2003 ; , normal inspection, Class II

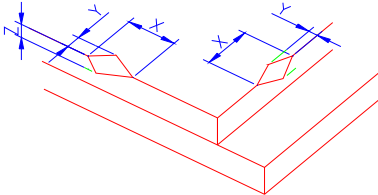
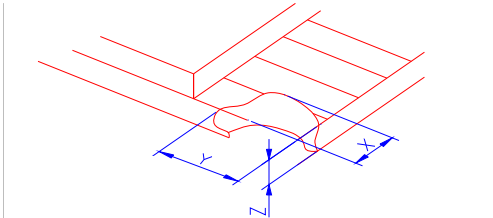
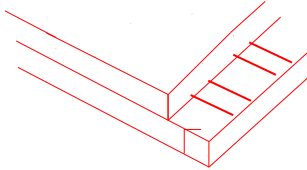
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

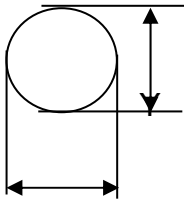
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot , Dim spot , Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

9.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

2.0

Spot defect



X

$$\Phi = (X + Y) / 2$$

① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.10$	Ignore		Ignore
$0.10 < \Phi \leq 0.25$	4(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.35$	3		
$\Phi > 0.4$	0		

② Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		Ignore
$0.10 < \Phi \leq 0.25$	4(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.35$	3		
$\Phi > 0.4$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.3 < \Phi \leq 0.5$	3(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	1		

④ Pixel bad points (light dot, Dim dot, color dot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.2 < \Phi \leq 0.3$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	1		

⑤ Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.3 < \Phi \leq 0.4$	4(distance ≥ 10 m)		
$0.4 < \Phi \leq 0.5$	3		
$\Phi > 0.5$	1		

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长期供货
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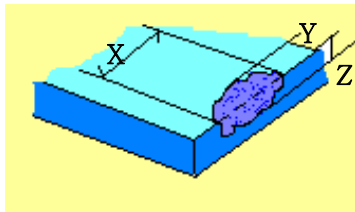
支持小量
NO MOQ

品种齐全
In Full Range

3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	Width(mm)	Length(m m)	Acceptable Qty		
				A	B	C
		$\Phi\leq0.05$	Ignore	Ignore		Ignore
		$0.05<W\leq0.06$	$L\leq4.0$	$N\leq3$		
		$0.07<W\leq0.08$	$L\leq3.0$	$N\leq2$		
		$0.08<W$	Define as spot defect			
4.0	Electronic Comp onents SMT	Not allow missing parts, solderless connection, cold solder joint, mis match, The positive and negative polarity opposite				
5.0	Display color& B rightness	1. Color: Measuring the color coordinates, The measurement standar d according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The meas urement standard according to the datasheet or Samples.				
6.0	LCD Mura	By 5% ND filter invisible.				

7.0	CTP Related	CTP Cover sensor accidented black/white spot				
			Size Φ (mm)	Acceptable Qty		
				A	B	C
			$\Phi \leq 0.1$	Ignore		Ignore
			$0.15 < \Phi \leq 0.25$	4 (distance ≥ 10 mm)		
			$0.25 < \Phi \leq 0.35$	3		
			$\Phi > 0.4$	1		

		<table><tr><td rowspan="6">CTP Cover scratch</td><td>Width(mm)</td><td>Ignore(mm)</td><td colspan="3">Acceptable Qty</td></tr><tr><td></td><td></td><td>A</td><td>B</td><td>C</td></tr><tr><td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="3">Ignore</td></tr><tr><td>$0.05 < W \leq 0.06$</td><td>$L \leq 4.0$</td><td colspan="3">$N \leq 3$</td></tr><tr><td>$0.07 < W \leq 0.08$</td><td>$L \leq 3.0$</td><td colspan="3">$N \leq 2$</td></tr><tr><td>$0.08 < W$</td><td colspan="4">Define as spot defect</td></tr></table>	CTP Cover scratch	Width(mm)	Ignore(mm)	Acceptable Qty					A	B	C	$\Phi \leq 0.05$	Ignore	Ignore			$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$			$0.07 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$			$0.08 < W$	Define as spot defect			
CTP Cover scratch	Width(mm)	Ignore(mm)		Acceptable Qty																													
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	$0.07 < W \leq 0.08$	$L \leq 3.0$		$N \leq 2$																													
	$0.08 < W$	Define as spot defect																															
CTP Cover Pinhole/ Lack of ink	<table><tr><td rowspan="6"> Zone Size (mm) </td><td colspan="3">Acceptable Qty</td></tr><tr><td colspan="3">C</td></tr><tr><td colspan="3">$\Phi \leq 0.2$</td></tr><tr><td colspan="3">Ignore</td></tr><tr><td colspan="3">$0.2 < \Phi \leq 0.3$</td></tr><tr><td colspan="3">4(distance $\geq 10\text{mm}$)</td></tr><tr><td colspan="3">$0.3 < \Phi \leq 0.4$</td></tr><tr><td colspan="3">3</td></tr><tr><td colspan="3">$\Phi > 0.4$</td></tr><tr><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			C			$\Phi \leq 0.2$			Ignore			$0.2 < \Phi \leq 0.3$			4(distance $\geq 10\text{mm}$)			$0.3 < \Phi \leq 0.4$			3			$\Phi > 0.4$			0			
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3																																	
$\Phi > 0.4$																																	
0																																	
CTP Bonding bubble/ accident spot	<table><tr><td rowspan="6">Size Φ(mm)</td><td colspan="2">Acceptable Qty</td></tr><tr><td>A</td><td>B</td></tr><tr><td colspan="2">$\Phi \leq 0.1$</td></tr><tr><td colspan="2">Ignore</td></tr><tr><td colspan="2">$0.15 < \Phi \leq 0.2$</td></tr><tr><td colspan="2">3(distance $\geq 10\text{mm}$)</td></tr><tr><td colspan="2">$0.2 < \Phi \leq 0.25$</td></tr><tr><td colspan="2">2</td></tr><tr><td colspan="2">$\Phi > 0.25$</td></tr><tr><td colspan="2">0</td></tr></table>	Size Φ (mm)	Acceptable Qty		A	B	$\Phi \leq 0.1$		Ignore		$0.15 < \Phi \leq 0.2$		3(distance $\geq 10\text{mm}$)		$0.2 < \Phi \leq 0.25$		2		$\Phi > 0.25$		0												
Size Φ (mm)	Acceptable Qty																																
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2																																	
$\Phi > 0.25$																																	
0																																	
Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																																
TP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X$\leq 0.5\text{mm}$</td><td>Y$\leq 0.5\text{mm}$</td><td>Z < cover thickness</td></tr></table> Circuitry broken is not allowed.	X	Y	Z	X $\leq 0.5\text{mm}$	Y $\leq 0.5\text{mm}$	Z < cover thickness																										
X	Y	Z																															
X $\leq 0.5\text{mm}$	Y $\leq 0.5\text{mm}$	Z < cover thickness																															

		TP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤0.3mm</td><td>Y≤0.3mm</td><td>Z<LCD thickness s</td></tr></table>	X	Y	Z	X≤0.3mm	Y≤0.3mm	Z<LCD thickness s	
X	Y	Z								
X≤0.3mm	Y≤0.3mm	Z<LCD thickness s								
* Circuitry broken is not allowed.										

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C, 96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Operating	+60°C, 90% RH, 96 hours.	
Thermal Shock (Non-operation)	-30°C, 30 min ↔ 80°C, 30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330, 5points/panel Air: ±8KV, 5times; Contact: ±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces, 80cm (MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

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11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

11.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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12. Packing

----TBD-----

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