



**SPECIFICATION
FOR
LCD Module
KD035HVFMA065-RT**

MODULE:	KD035HVFMA065-RT
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2017.05.20

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5" TFT-LCD contains 320x480 pixels, and can display up to 65K/262K colors.

* Features

- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K colors
- Interface: 8/9/16/18BIT MCU Interface
3/4SPI+16/18Bit RGB Interface

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.96(H)*73.44 (V) (3.5inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*480	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ILI9488	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		55.50		mm	-
	Vertical(V)		84.96		mm	-
	Depth(D)		3.7		mm	-
Weight			TBD		g	-

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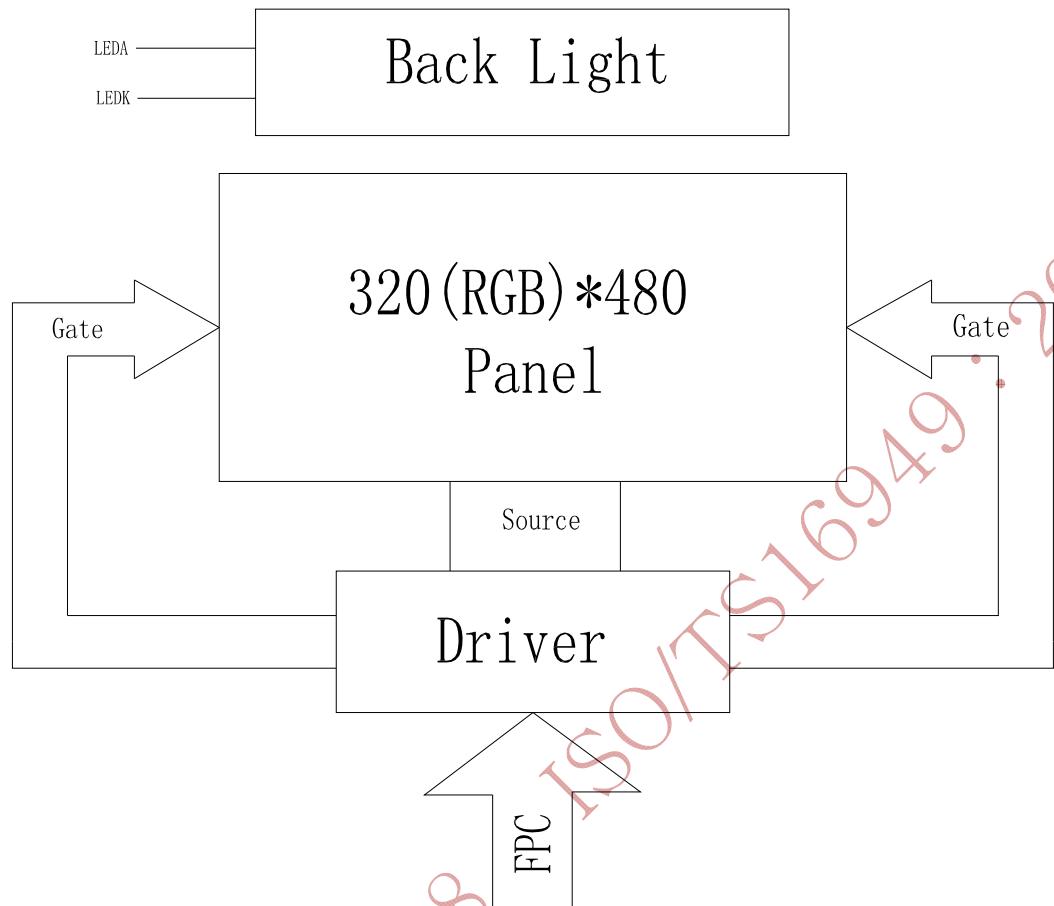
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1. Block Diagram



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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION					I/O																																																
1	GND	Ground.					P																																																
2	XR	Touch panel Right Glass Terminal					A/D																																																
3	YD	Touch panel Bottom Film Terminal					A/D																																																
4	XL	Touch panel LIFT Glass Terminal					A/D																																																
5	YU	Touch panel Top Film Terminal					A/D																																																
6	IOVCC	I/O power supply voltage.					P																																																
7	VCC	Supply Voltage (3.3V).					P																																																
8	IM0	<table><tr><th colspan="6">Interface Selection</th></tr><tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th colspan="2">DB Pin in use</th></tr><tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 18-bit interface</td><td colspan="2">DB17-DB0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_ 9-bit interface</td><td colspan="2">DB8-DB0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_ 16-bit interface</td><td colspan="2">DB15-DB0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_ 8-bit interface</td><td colspan="2">DB7-DB0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 BIT data serial interface</td><td colspan="2">SDI SCL CS</td></tr><tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 BIT data serial interface</td><td colspan="2">SDI SCL CS RS</td></tr></table>					Interface Selection						IM2	IM1	IM0	Interface type	DB Pin in use		0	0	0	DBI Tyb_ 18-bit interface	DB17-DB0		0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0		0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0		0	1	1	DBI Tyb_ 8-bit interface	DB7-DB0		1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS		1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS		I
Interface Selection																																																							
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1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS																																																			
9	IM1																																																						
10	IM2																																																						
11	RESET	Reset input signal Initialize the chip with a low input. Be sure to execute a power-on reset after supplying power.					I																																																
12	VSYNC	Frame synchronizing signal Fix to DGND level when not in use.					I																																																
13	HSYNC	Line synchronizing signal Fix to DGND level when not in use.					I																																																
14	PCLK	Dot clock signal Fix to DGND level when not in use.					I																																																
15	DE	A data ENABLE input signal Fix to DGND level when not in use.					I																																																
16-33	DB17-DB0	18-bit data bus.					I/O																																																
		RGB Interface Type			Data PIN in Use																																																		
		16 BIT RGB			DB0-DB15																																																		
		18 BIT RGB			DB0-DB17																																																		



		Fix to GND level when not in use	
34	SDO	Serial data output Leave the pin open when not in use.	O
35	SDA	DIN/SDA: serial data input/output bi-direction pin Fix to DGND level when not in use.	I
36	RD	serve as a read signal Fix to IOVCC level when not in use.	I
37	WR(SCL)	WRX pin, serves as a write signal SCL pin as Serial Clock when operates in the serial interface Fix to IOVCC level when not in use.	I
38	RS	Data/Command Selection pin Low: Command High: Parameter Fix to IOVCC level when not in use.	I
39	CS	Chip select input signal Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to IOVCC level when not in use.	I
40	GND	Ground.	P
41-48	LEDK8-LEDK1	Cathode pin OF backlight	P
49	LEDA	Anode pin of backlight	P
50	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	--	500	--		NOTE2
Response time	Rising	T_{R+T_F}		--	35	50	msec	NOTE4
	Falling							
Uniformity		S(%)		--	70	--	%	NOTE1
Color Filter Chromaticity	White	W_X		0.288	0.328	0.368		
		W_Y		0.348	0.388	0.428		
	Red	R_X		0.615	0.635	0.655		
		R_Y		0.317	0.337	0.357		
	Green	G_X		0.300	0.320	0.340		
		G_Y		0.615	0.635	0.655		
	Blue	B_X		0.137	0.157	0.177		
		B_Y		0.021	0.041	0.061		
Viewing angle	Hor.	Θ_L	CR>10	--	80	--		NOTE5
		Θ_R		--	80	--		
	Ver.	Θ_U		--	80	--		
		Θ_D		--	80	--		
		Option View Direction		Free				

Note 1 Uniformity

$$\text{Uniformity of 9 points} = \frac{\text{Min Luminance of Y1~Y9}}{\text{Max Luminance of Y1~Y9}} \times 100\%$$

Note 2 Contrast Ratio (CR)

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

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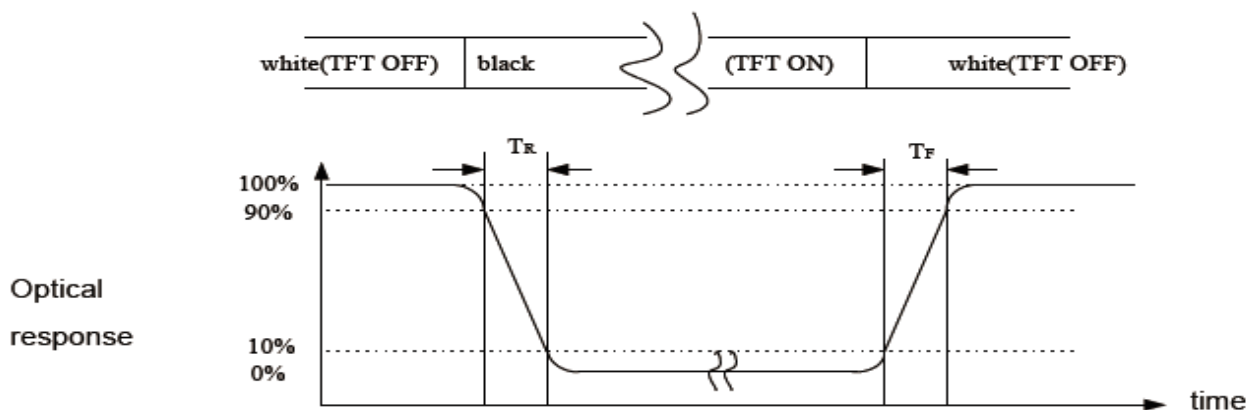
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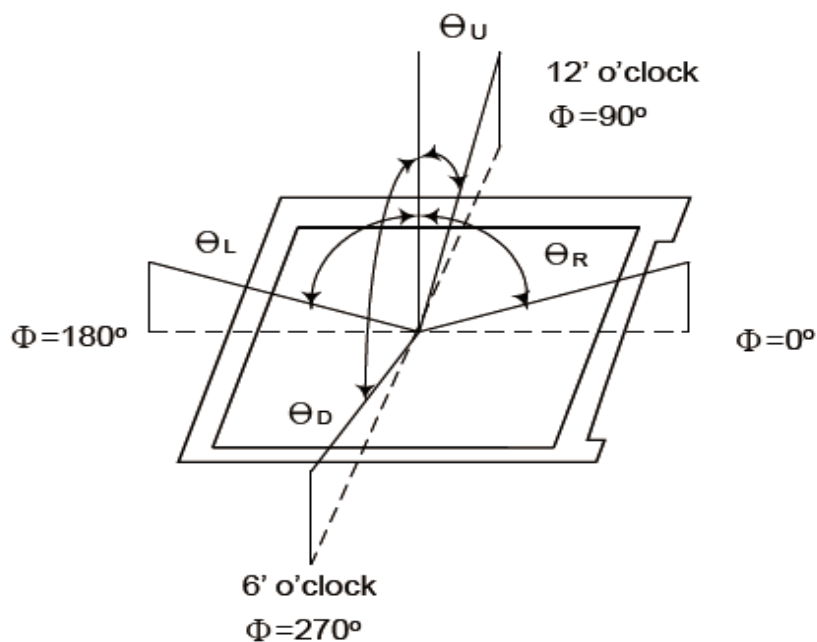
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Note 4 Response Time



Note 5 View Angle



ISO9001

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5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	V _{CI}	-0.3	6.0	V
Digital interface supply Voltage	IOVCC	-0.3	3.3	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.5	2.8	3.3	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V _{IH}	0.7IOVCC		IOVCC	V	
	V _{IL}	GND		0.3IOVCC	V	
Level output voltage	V _{OH}	0.8IOVCC		IOVCC	V	
	V _{OL}	GND		0.2IOVCC	V	

5.3 LED Backlight Characteristics

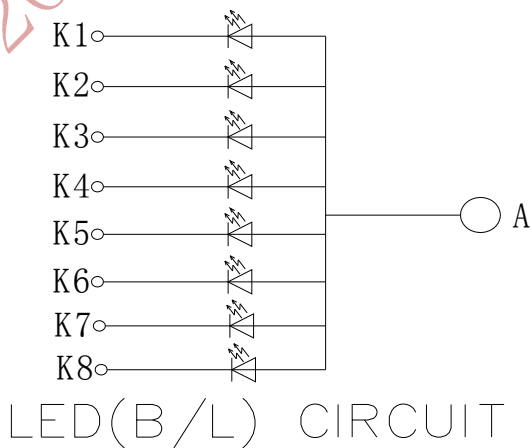
The back-light system is edge-lighting type with 8chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	150	160	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_v	286	336	--	cd/m ²	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

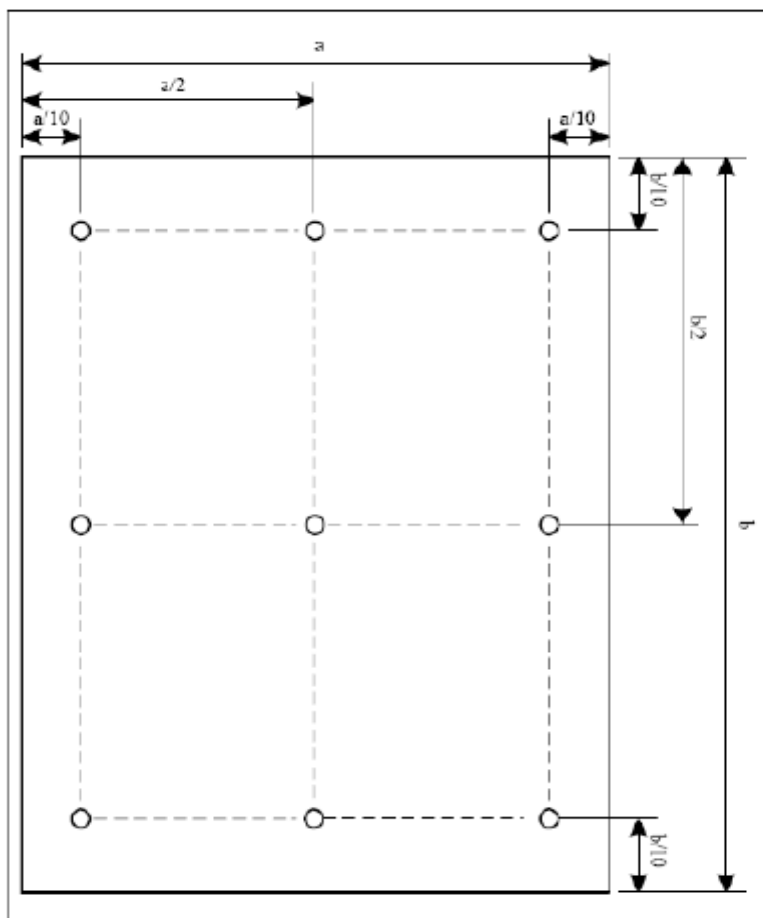
$T_a = 25 \pm 3^\circ \text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at $T_a = 25^\circ \text{C}$ and $I_L = 160 \text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 160mA. The constant current driving method is suggested.





NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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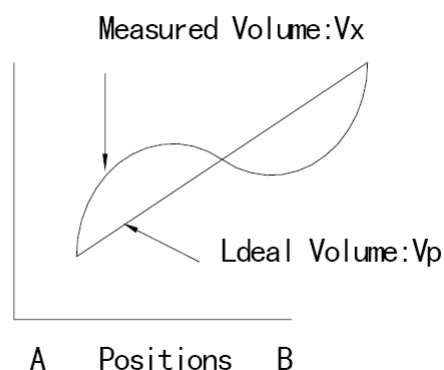
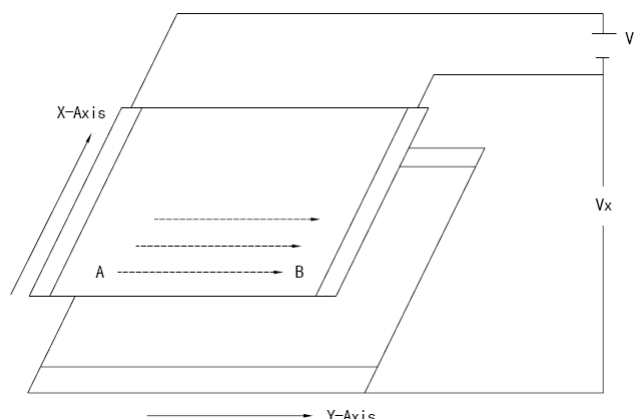
6. TP Feature

6.1 Conditions of use and storage

Item	Value(condition)	Note
Temperature range upon operation	Humidity: 20%~90% non dew, condensation -20℃~70℃	In a simple substance
Temperature range upon storage	Humidity: 20%~90% non dew, condensation -30℃~80℃	In a simple substance

6.2 Electrical property

Item	Value	Note
Maximum voltage	DC5V	
Resistance between terminals	X direction[Film side]:200-600Ω Y direction [Glass side]:300-900Ω	
Insulation resistance	DC 25V 20MΩor above	Connect X + ~X- and Y+ ~Y-, apply 25VDC Between X and Y for perform measurements
Chattering	10 msec or below	
Rating	Voltage is DC 5V	



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6.3 Mechanical property

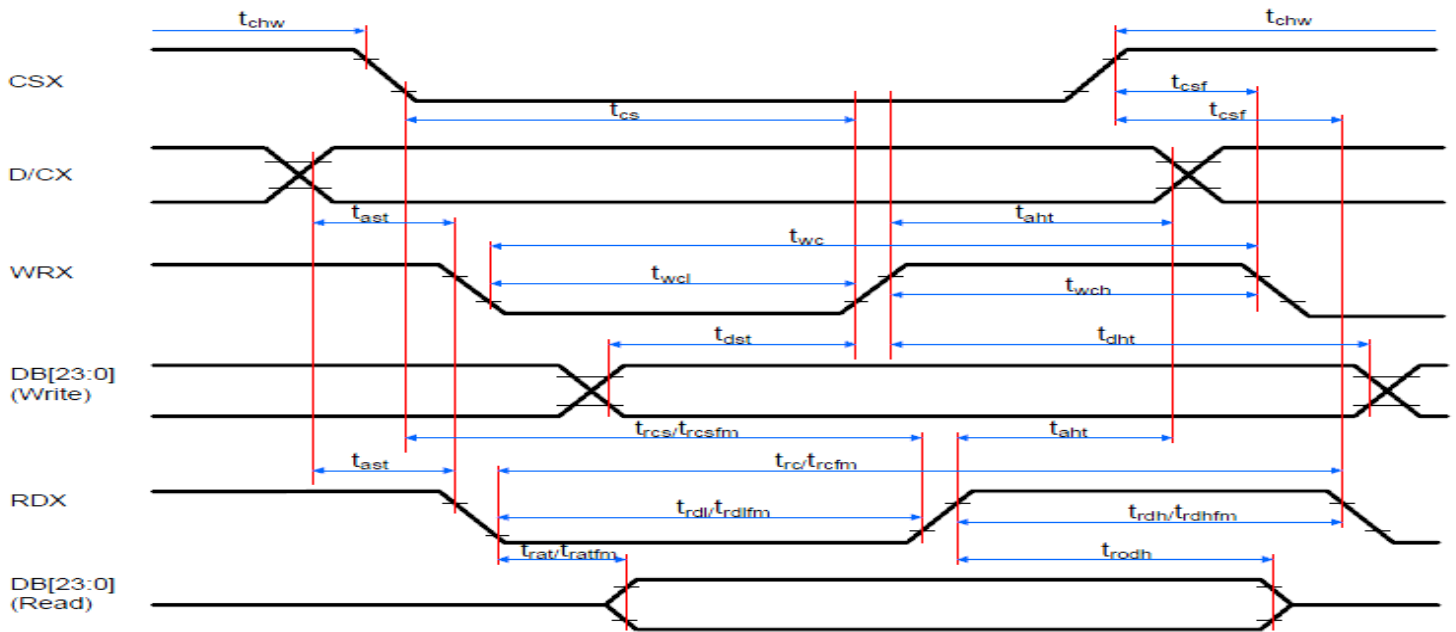
Item	Performance		Note
Input method	Used of an exclusive pen or finger		
Load upon operation	Exclusive pen	60-100g or below	Operation and measurement with a pen must be carried out under the following tip condition s: Stylus pen material : POM(ployacetal) . Tip : Diameter 3.0mm, SR 0.8 mm
	Finger	60-100g or below	Operations and measurement methods simulate d for a finger must be carried out under the fo llowing tip conditions. Material :Silicon rubber (Hardness : 30°Hs) Tip : Diameter 12.0 mm, SR 12.5mm
Surface hardness	Pencil hardness : 3H or above		It complies with the way of test method JIS K5400.

6.4 Optical property

Item	Performance	Note
Total light transmittance	80% or above	JIS K7105
Haze	5% or below	JIS K7136
Film specification	Polished type with hard coated surface	

7. AC Characteristic

7.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)

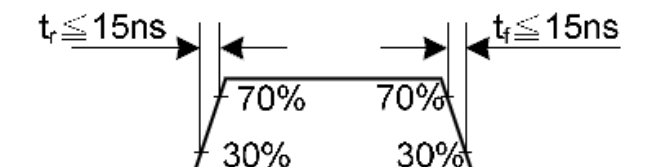


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchwh	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

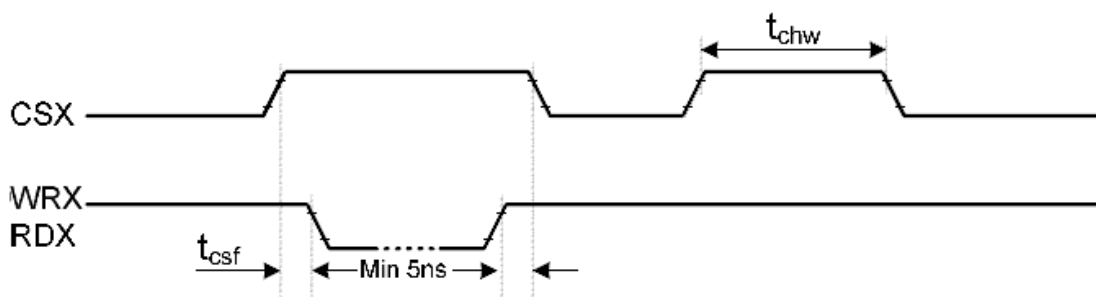


Notes:

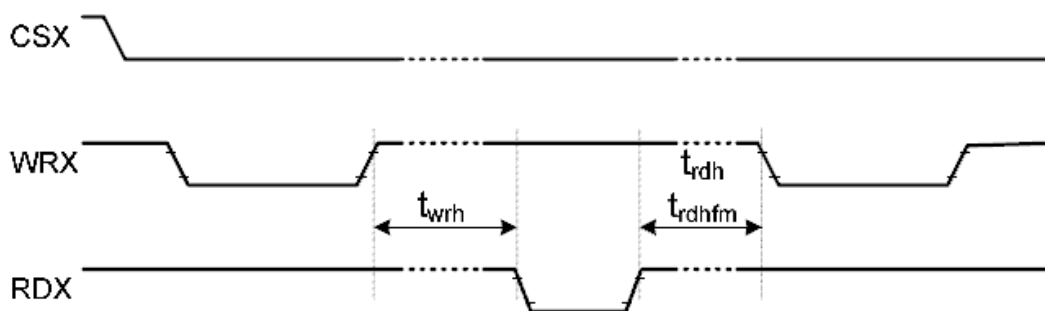
1. $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $\text{IOVCC} = 1.65\text{V}$ to 3.3V , $\text{VCI} = 2.5\text{V}$ to 3.3V , $\text{AGND} = \text{DGND} = 0\text{V}$
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:



5. The Write to Read or the Read to Write timing:



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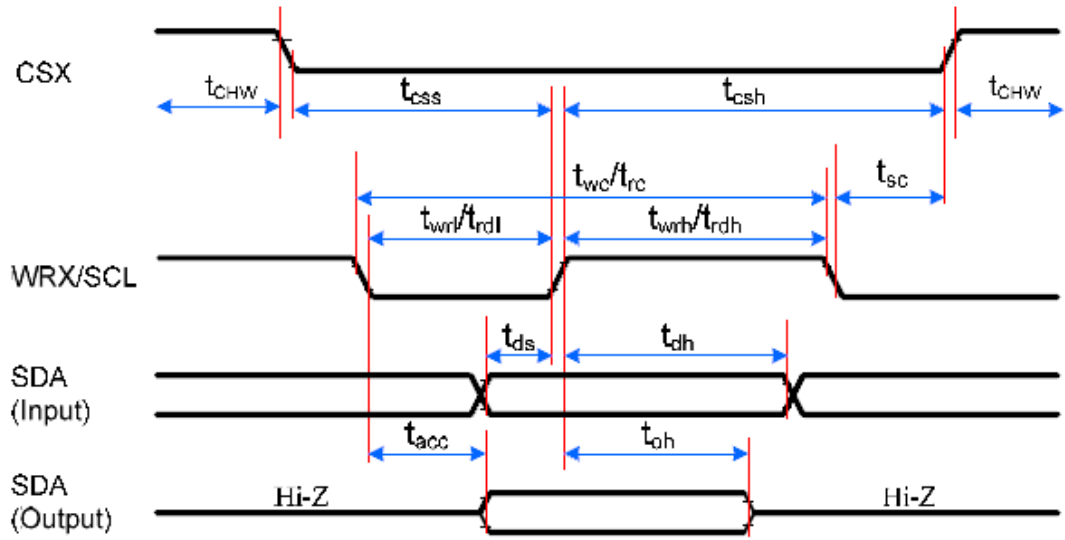
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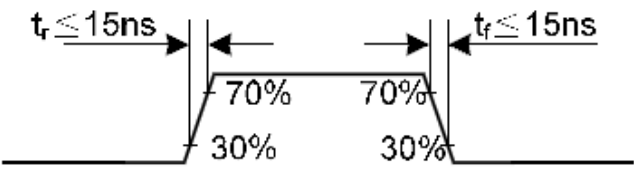
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7.2 Display Serial Interface Timing Characteristics (3-line SPI system)

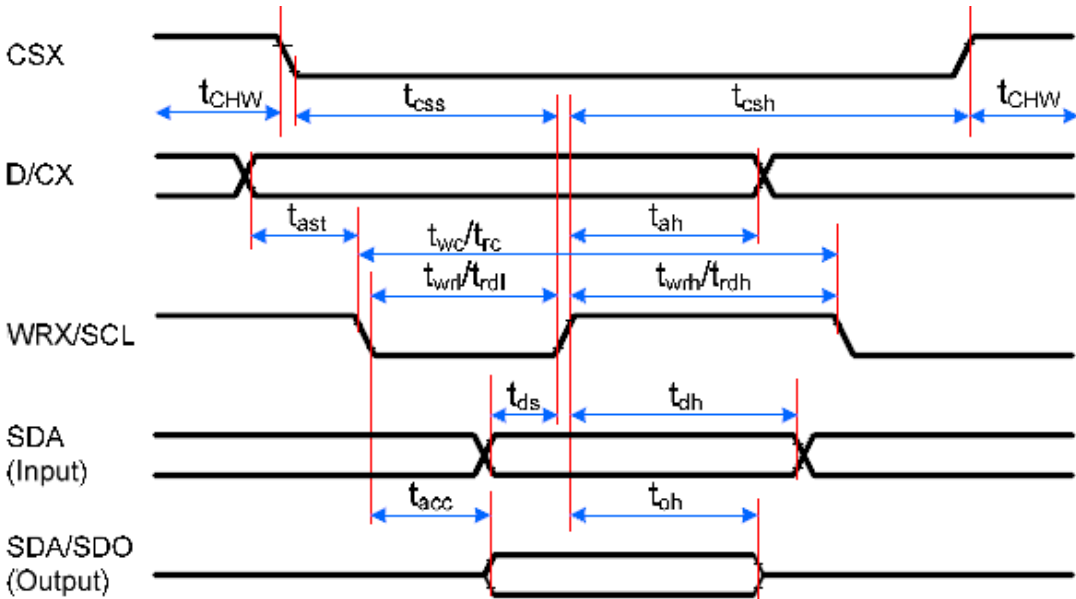


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchwh	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



7.3 Display Serial Interface Timing Characteristics (4-line SPI system)

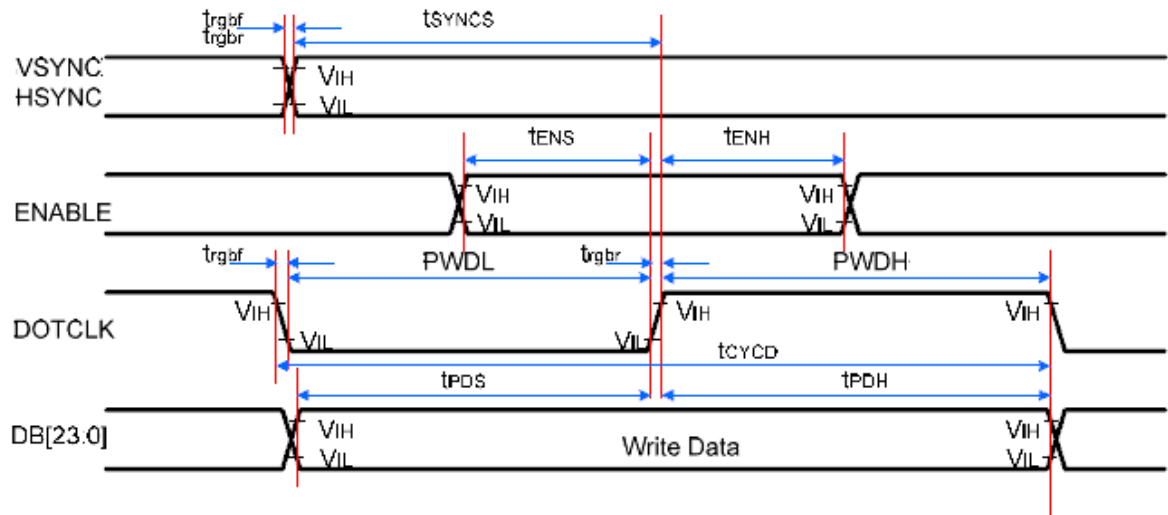


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	15	-	ns	
	t_{csh}	Chip select hold time (Read)	15	-	ns	
	t_{CHW}	CS H pulse width	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	50	-	ns	
	t_{wrh}	SCL H pulse width (Write)	10	-	ns	
	t_{wrl}	SCL L pulse width (Write)	10	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL H pulse width (Read)	60	-	ns	
	t_{rdl}	SCL L pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-	ns	
	t_{ah}	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	t_{ds}	Data setup time (Write)	10	-	ns	
	t_{dh}	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	t_{acc}	Access time (Read)	10	50	ns	For maximum CL=30pF
	t_{od}	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Notes:

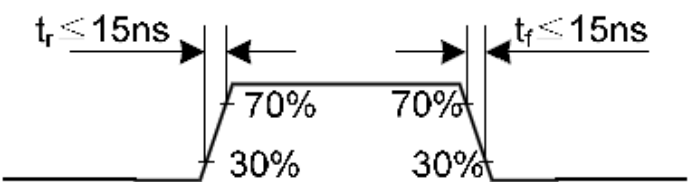
- $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $\text{IOVCC} = 1.65\text{V}$ to 3.3V , $\text{VCI} = 2.5\text{V}$ to 3.3V , $\text{AGND} = \text{DGND} = 0\text{V}$, $T = 10\pm 0.5\text{ns}$.
- Does not include signal rising and falling times.

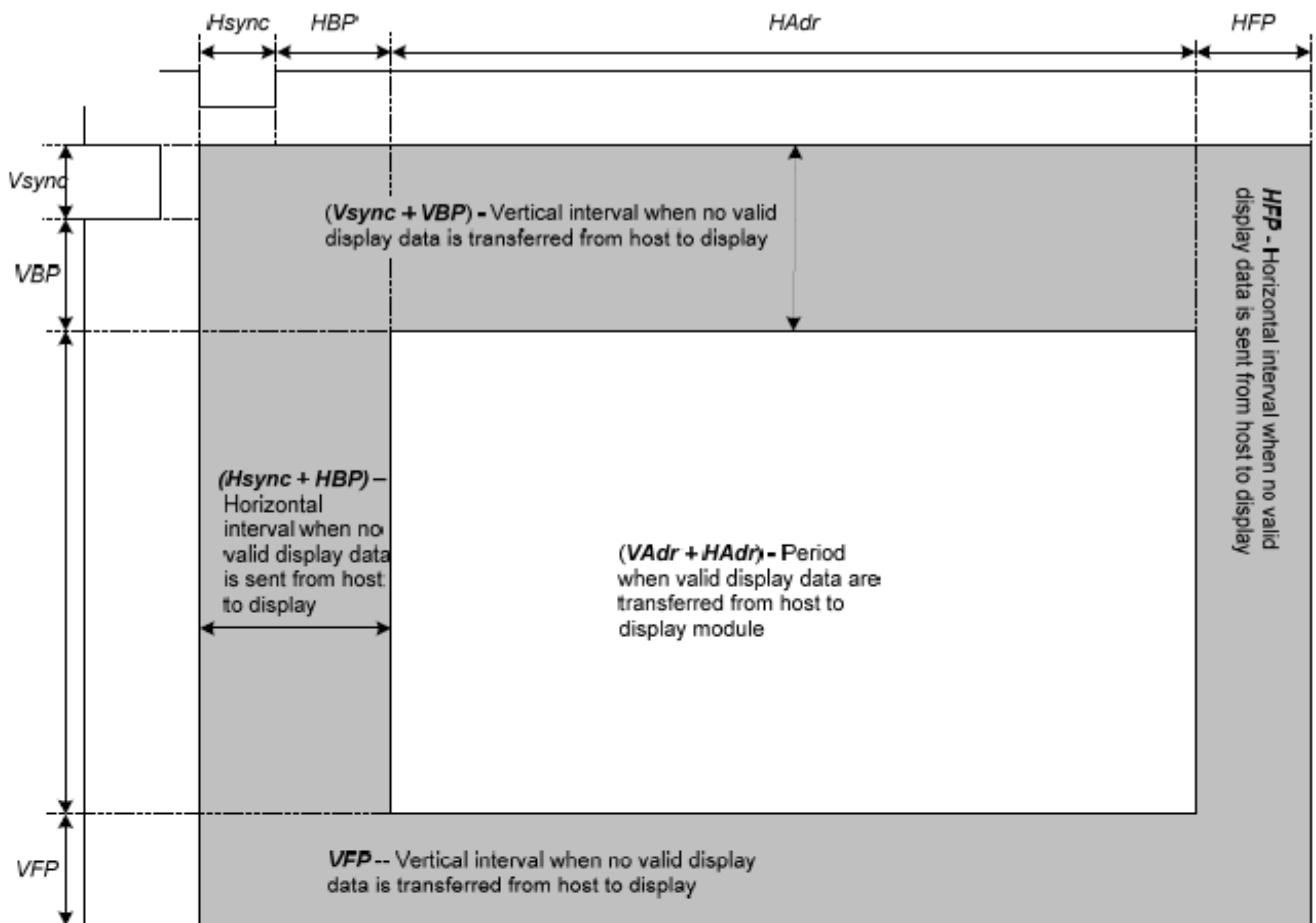
7.4 Parallel RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	$t_{rgb\uparrow}, t_{rgb\downarrow}$	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V





Parameters	Symbols	Min.	Typ.	Max.	Units
PCLK Cycle	PCLK _{CYC}	100	80	66.6	ns
Horizontal Synchronization	Hsync	3	3	-	PCLK
Horizontal Back Porch	HBP	3	3	-	PCLK
Horizontal Address	HAdr	-	320	-	PCLK
Horizontal Front Porch	HFP	3	3	-	PCLK
Vertical Synchronization	Vsync	2	2	-	Line
Vertical Back Porch	VBP	2	2	-	Line
Vertical Address	VAdr	-	480	-	Line
Vertical Front Porch	VFP	2	2	-	Line
Vertical Frequency(*)		50	60	80	Hz
Horizontal Frequency(*)		-	33	-	KHz
PCLK Frequency(*)		10	12.5	15	MHz

- Notes:
- Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
 - Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
 - Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

7.5 Reset Timing Characteristics

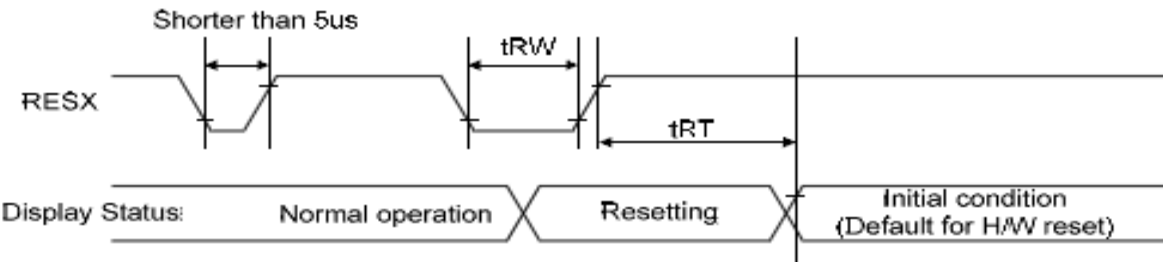


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

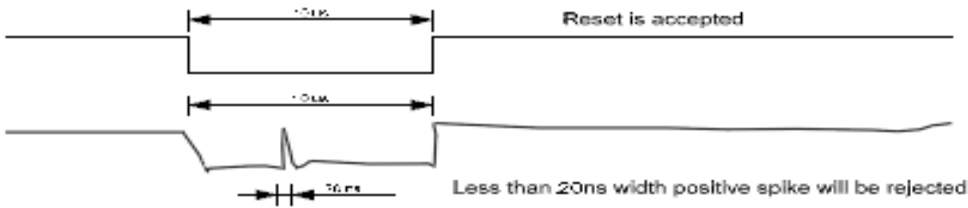


Figure 137: Positive Noise Pulse during Reset Low

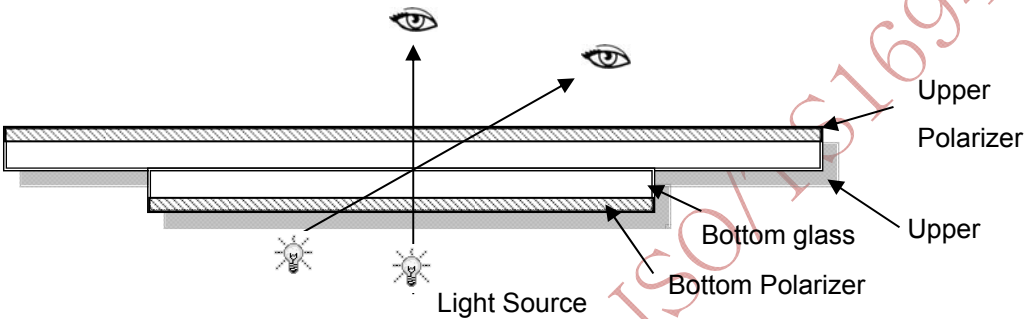
8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

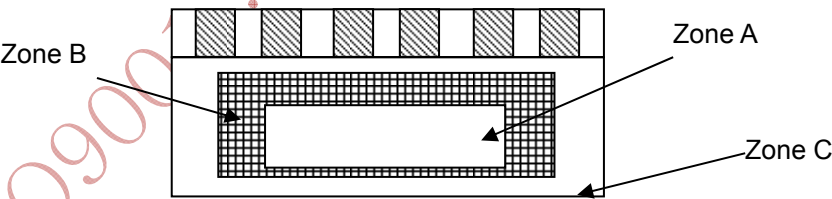
8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



8.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

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常备库存 Stock For Sale		长期供货 Long Time supply		支持小量 NO MOQ
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8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

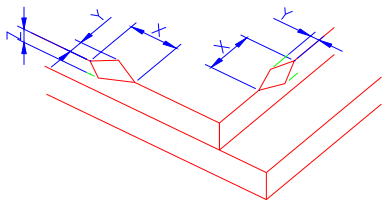
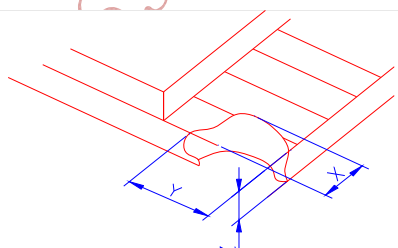
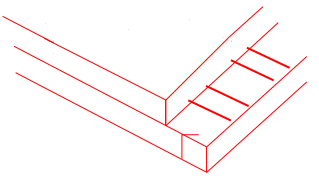
AQL:

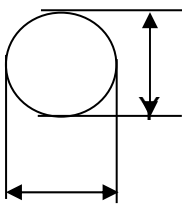
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
		(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L
X	Y	Z						
≤3.0mm	≤L	≤T						
	(3) LCD crack	 Crack Not allowed						

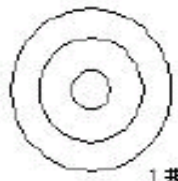
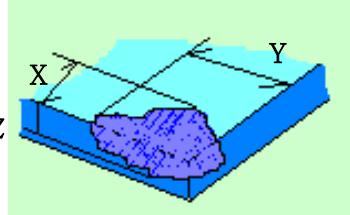
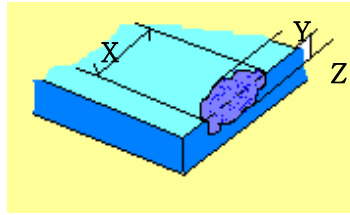
Number	Items	Criteria (mm)																									
2.0	Spot defect  X Φ=(X+Y)/2	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)																									
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Accep able Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.30</td><td colspan="2">Ignore</td><td rowspan="4">Ignor</td></tr><tr><td>0.20<Φ≤0.3</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.25<Φ≤0.35</td><td colspan="2">2</td></tr><tr><td>Φ > 0.4</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Accep able Qty			A	B	C	Φ≤0.30	Ignore		Ignor	0.20<Φ≤0.3	3(distance ≥ 10mm)		0.25<Φ≤0.35	2		Φ > 0.4	0						
		Zone Size (mm)		Accep able Qty																							
			A	B	C																						
		Φ≤0.30	Ignore		Ignor																						
		0.20<Φ≤0.3	3(distance ≥ 10mm)																								
		0.25<Φ≤0.35	2																								
		Φ > 0.4	0																								
		②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)																									
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.3</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.2<Φ≤0.3</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.25<Φ≤0.35</td><td colspan="2">2</td></tr><tr><td>Φ > 0.4</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.3	Ignore		Ignore	0.2<Φ≤0.3	3(distance ≥ 10mm)		0.25<Φ≤0.35	2		Φ > 0.4	0						
		Zone Size (mm)		Acceptable Qty																							
			A	B	C																						
		Φ≤0.3	Ignore		Ignore																						
		0.2<Φ≤0.3	3(distance ≥ 10mm)																								
		0.25<Φ≤0.35	2																								
	Φ > 0.4	0																									
	③ Polarizer accidented spot																										
	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.3</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.25<Φ≤0.5</td><td colspan="2">2(distance ≥ 10mm)</td></tr><tr><td>Φ>0.5</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.3	Ignore		Ignore	0.25<Φ≤0.5	2(distance ≥ 10mm)		Φ>0.5	0										
	Zone Size (mm)		Acceptable Qty																								
		A	B	C																							
	Φ≤0.3	Ignore		Ignore																							
0.25<Φ≤0.5	2(distance ≥ 10mm)																										
Φ>0.5	0																										
Line defect (LCD/TP/Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.05</td><td>Igno e</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.04<W≤0.07</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr><tr><td>0.06<W≤0.09</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr><tr><td>0.09<W</td><td colspan="4">Define as spot defect</td></tr></table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.05	Igno e	Ignore		Ignore	0.04<W≤0.07	L≤3.0	N≤2		0.06<W≤0.09	L≤2.0	N≤2		0.09<W	Define as spot defect			
	Width(mm)			Length(mm)	Acceptable Qty																						
		A	B		C																						
	Φ≤0.05	Igno e	Ignore		Ignore																						
	0.04<W≤0.07	L≤3.0	N≤2																								
	0.06<W≤0.09	L≤2.0	N≤2																								
	0.09<W	Define as spot defect																									



3.0	Polarizer Bubble	Zone Size (mm)	Acceptable Qty		
			A	B	C
		$\Phi \leq 0.2$	Ignore		Ignore
		$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 m)		
		$0.4 < \Phi \leq 0.6$	2		
		$0.6 < \Phi$	0		

4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.
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		TP bubble/ accidented spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.3$</td><td colspan="3">Ignore</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td colspan="3">3 (distance $\geq$</td></tr><tr><td>$0.25 < \Phi \leq 0.35$</td><td colspan="3">2</td></tr><tr><td>$0.4 < \Phi$</td><td colspan="3">0</td></tr></table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.3$	Ignore			$0.25 < \Phi \leq 0.3$	3 (distance $\geq$			$0.25 < \Phi \leq 0.35$	2			$0.4 < \Phi$	0		
Size Φ (mm)	Acceptable Qty																											
	A		B	C																								
$\Phi \leq 0.3$	Ignore																											
$0.25 < \Phi \leq 0.3$	3 (distance $\geq$																											
$0.25 < \Phi \leq 0.35$	2																											
$0.4 < \Phi$	0																											
		Assembly deflection	beyond the edge of backlight $\leq 0.15\text{mm}$																									

5.0	TP Related	Newton Ring Newton Ring area>1/3 TP area NG Newton Ring area≤1/3 TP area OK	 1 规律性  2 非规律性  似牛顿环						
	TP corner broken X : length Y : width Z : height *	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thicknes</td></tr></table> Circuitry broken is not allowed.	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thicknes	
X	Y	Z							
X≤3.0mm	Y≤3.0mm	Z<LCD thicknes							
	TP edge broken X : length Y : width Z : height *	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thicknes	
X	Y	Z							
X≤6.0mm	Y≤2.0mm	Z<LCD thicknes							

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	-30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω, ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

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				品种齐全 In Full Range

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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11. Packing

---TBD-----

ISO9001 : 2008 ISO/TS16949 : 2009

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