



**SPECIFICATION
FOR
LCD+CTP Module
KD024C-4-C003A**

MODULE:	KD024C-4-C003A
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2016.04.28

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PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
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常备库存
Standing Stock

长期供货
Long Time supply

支持小量
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ISO9001 : 2008

ISO/TS16949 : 2009

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.4'TFT-LCD contains 240x320 pixels, and can display up to 65K/262K colors.

* Features

- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K colors
- TFT Interface: 8/9/16/18Bit MCU Interface
3/4SPI+16/18Bit RGB Interface
3-line/4-line Serial Interface
- CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	36.72(H)*48.96(V) (2.4inch)	mm	-
CTP View area	42.62(H)*49.56(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*320	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	12:00	o'clock	-
TFT Controller IC	ST7789V	-	-
CTP Driver IC	FT6336G	-	-
Display mode	Transmissive/Normally Black	-	-
Touch mode	Single point and Gestures	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		42.72		mm	-
	Vertical(V)		60.26		mm	-
	Depth(D)		3.85		mm	-
Weight			TBD		g	-

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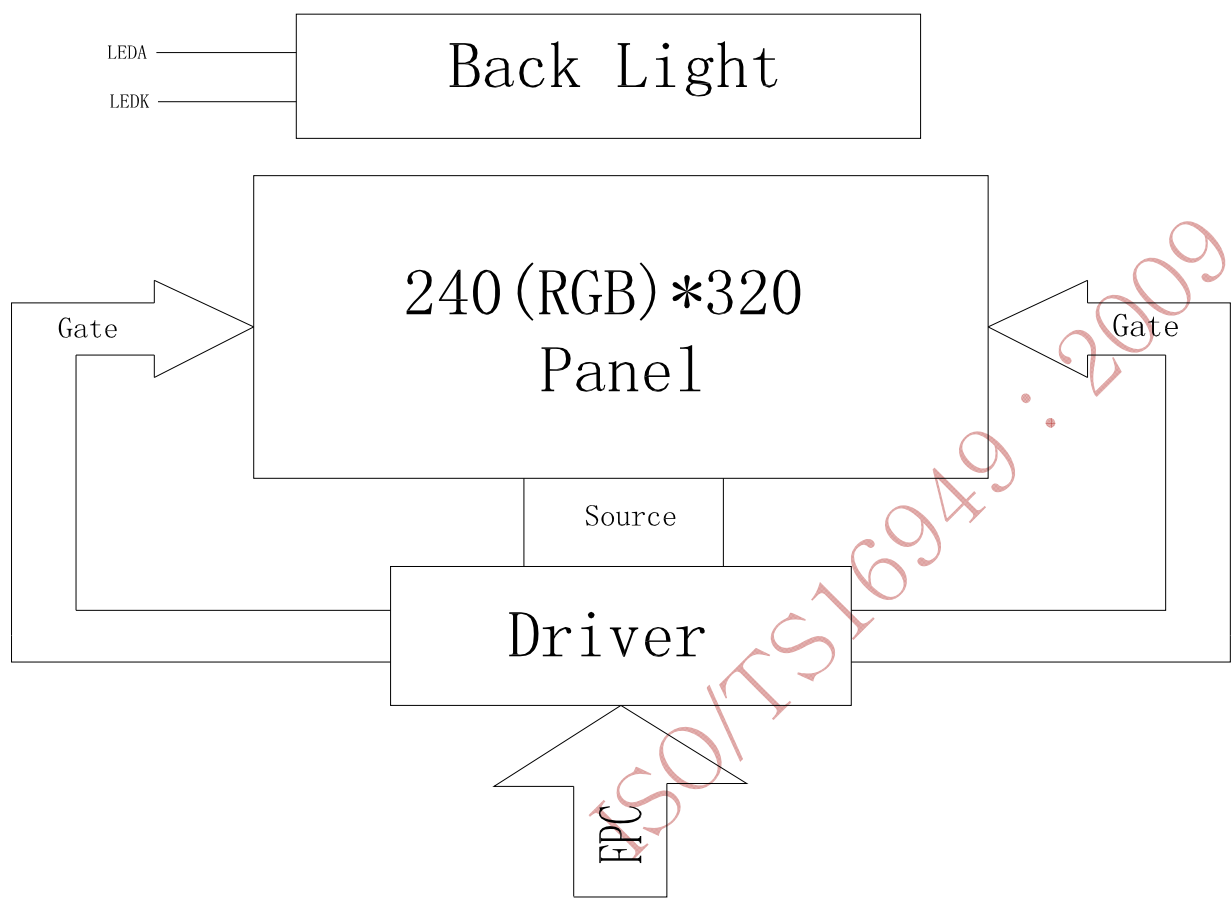
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1. Block Diagram





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3. Input terminal Pin Assignment

3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VCI	Supply Voltage (3.3V).	P
3	VCI	Supply Voltage (3.3V).	P
4	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.	I
5	IM1		I
6	IM0		I
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin ("Low" enable). Fix this pin at VCI or GND when not in use.	I
9	DC(SPI-SCL)	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. Fix this pin at VCI or GND when not in use.	I
10	WR(SPI-RS)	The data is applied on the rising edge of the SCL signal. If not used, Fix this pin at VCI or GND when not in use.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at VCI or GND when not in use.	I
12	VSYN	Frame synchronizing signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
13	HSYN	Line synchronizing signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
14	ENABLE	Data enable signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
15	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
16	SDA	Serial input signal. The data is latched on the rising edge of the SCL signal. Fix this pin at VCI or GND when not in use.	I

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17-34	DB0-DB17	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND level when not in use	I/O
35	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
36	LEDA	Anode pin of backlight	P
37	LEDK1	Cathode pin OF backlight	P
38	LEDK2	Cathode pin OF backlight	P
39	LEDK3	Cathode pin OF backlight	P
40	LEDK4	Cathode pin OF backlight	P
41	XR	Touch panel Right Glass Terminal	A/D
42	YU	Touch panel Bottom Film Terminal	A/D
43	XL	Touch panel LIFT Glass Terminal	A/D
44	YD	Touch panel Top Film Terminal	A/D
45	GND	Ground.	P

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

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4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	--	250			
Response time		T_R+T_F		--	30	--	msec	
Color gamut		S(%)		--	70	--	%	
Color Filter Chromaticity	White	W_X		0.288	0.308	0.328		
		W_Y		0.305	0.325	0.345		
	Red	R_X		0.592	0.612	0.632		
		R_Y		0.309	0.329	0.349		
	Green	G_X		0.279	0.299	0.319		
		G_Y		0.547	0.567	0.587		
	Blue	B_X		0.124	0.144	0.164		
		B_Y		0.090	0.110	0.130		
Viewing angle	Hor.	Θ_L	CR>10	--	45	--		
		Θ_R		--	45	--		
	Ver.	Θ_U		--	45	--		
		Θ_D		--	20	--		
		Option View Direction		Free				

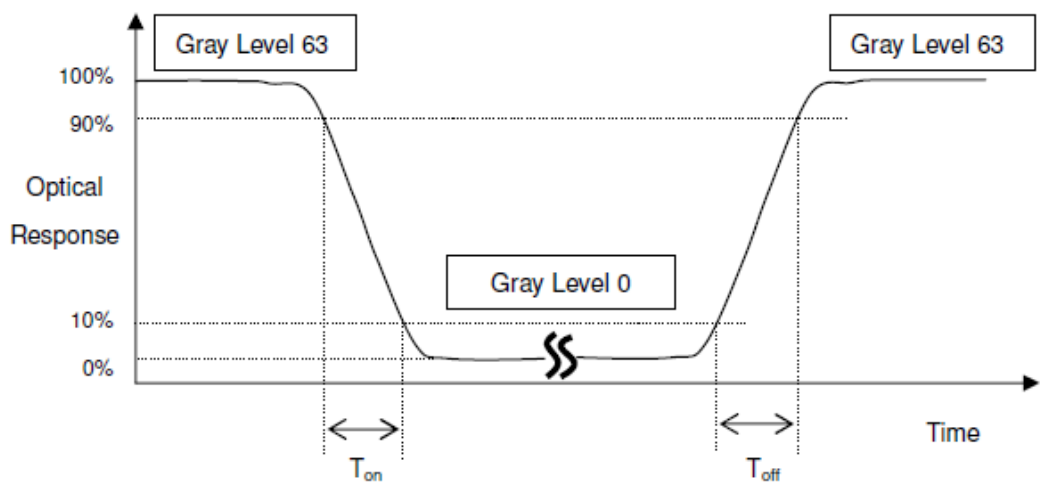
4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25\pm 2^\circ\text{C}$
- 15min. warm-up time.

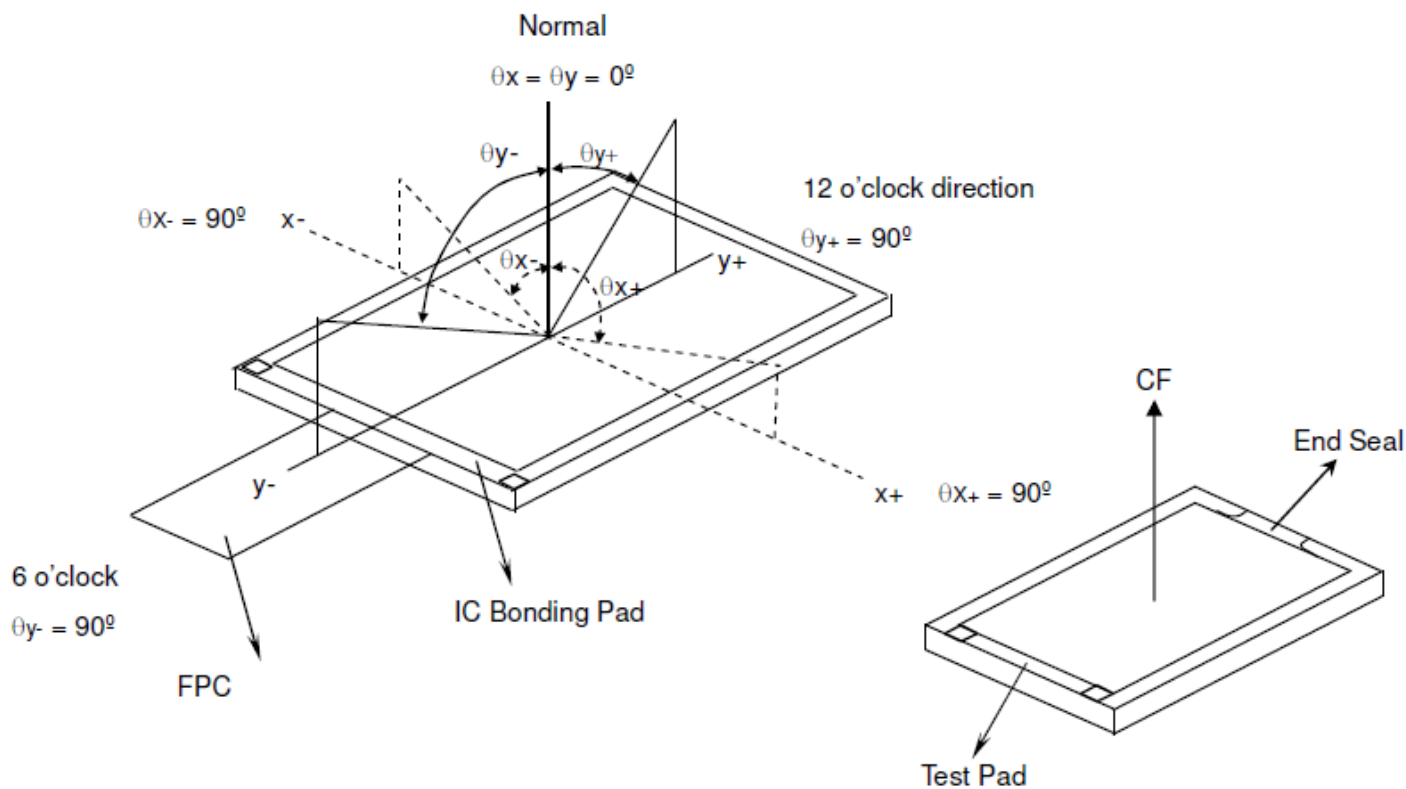


4.3 Measuring Equipment

*Note (2) Definition of Response Time (T_{on} , T_{off}):



*Note (3) Definition of Viewing Angle

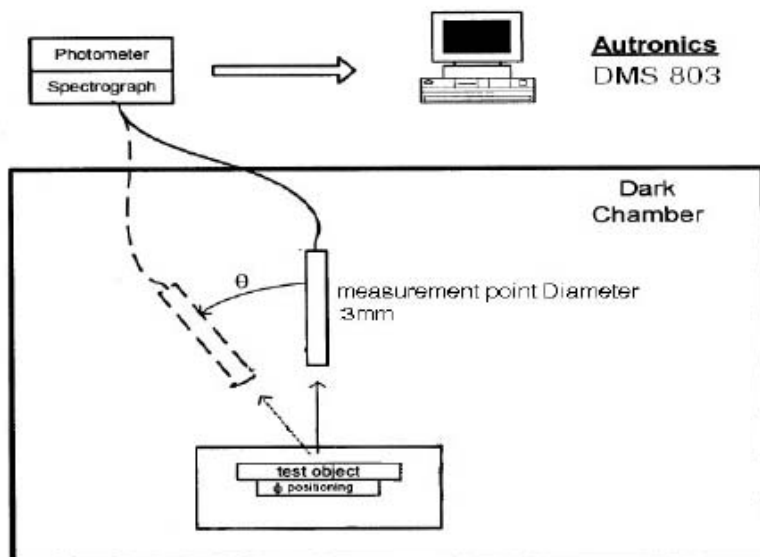


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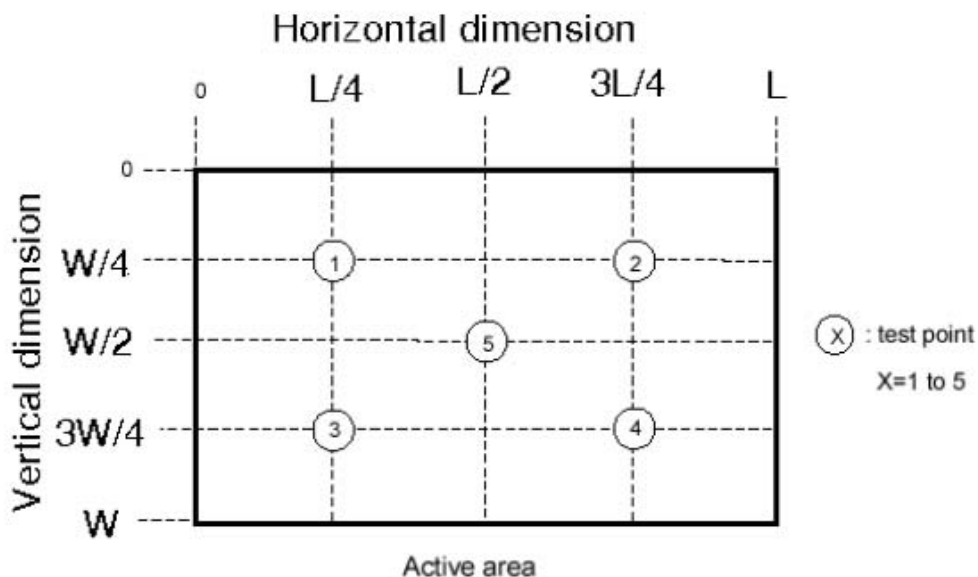


*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



*Note (5)



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5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI/VDD	2.4	3.3	V
Digital interface supply Voltage	IOVCC	1.65	3.3	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI/VDD	2.4	--	3.3	V	
Digital interface supply Voltage	IOVCC	1.65	--	3.3	V	
Normal mode Current consumption	IDD	--	7	--	mA	
Level input voltage	V _{IH}	0.7V _{DDIO}		V _{DDIO}	V	
	V _{IL}	GND		0.3V _{DDIO}	V	
Level output voltage	V _{OH}	0.8V _{DDIO}		V _{DDIO}	V	
	V _{OL}	GND		0.2V _{DDIO}	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	60	80	--	mA	
Forward Voltage	V _F	--	3.2	--	V	
LCM Luminance	L _V	210	--	--	cd/m ²	If=60mA
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	

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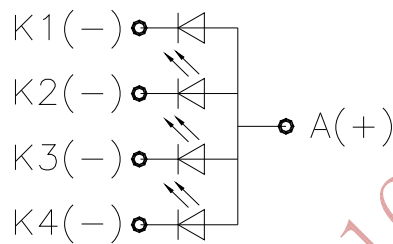


Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a = 25 \pm 3^\circ\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at

$T_a = 25^\circ\text{C}$ and $I_L = 60\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 60mA. The constant current driving method is suggested.



BLU CIRCUIT DIAGRAM

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6. AC Characteristic

6.1 8080 Series MCU Parallel Interface Timing Characteristics: 18/16/9/8-bit Bus

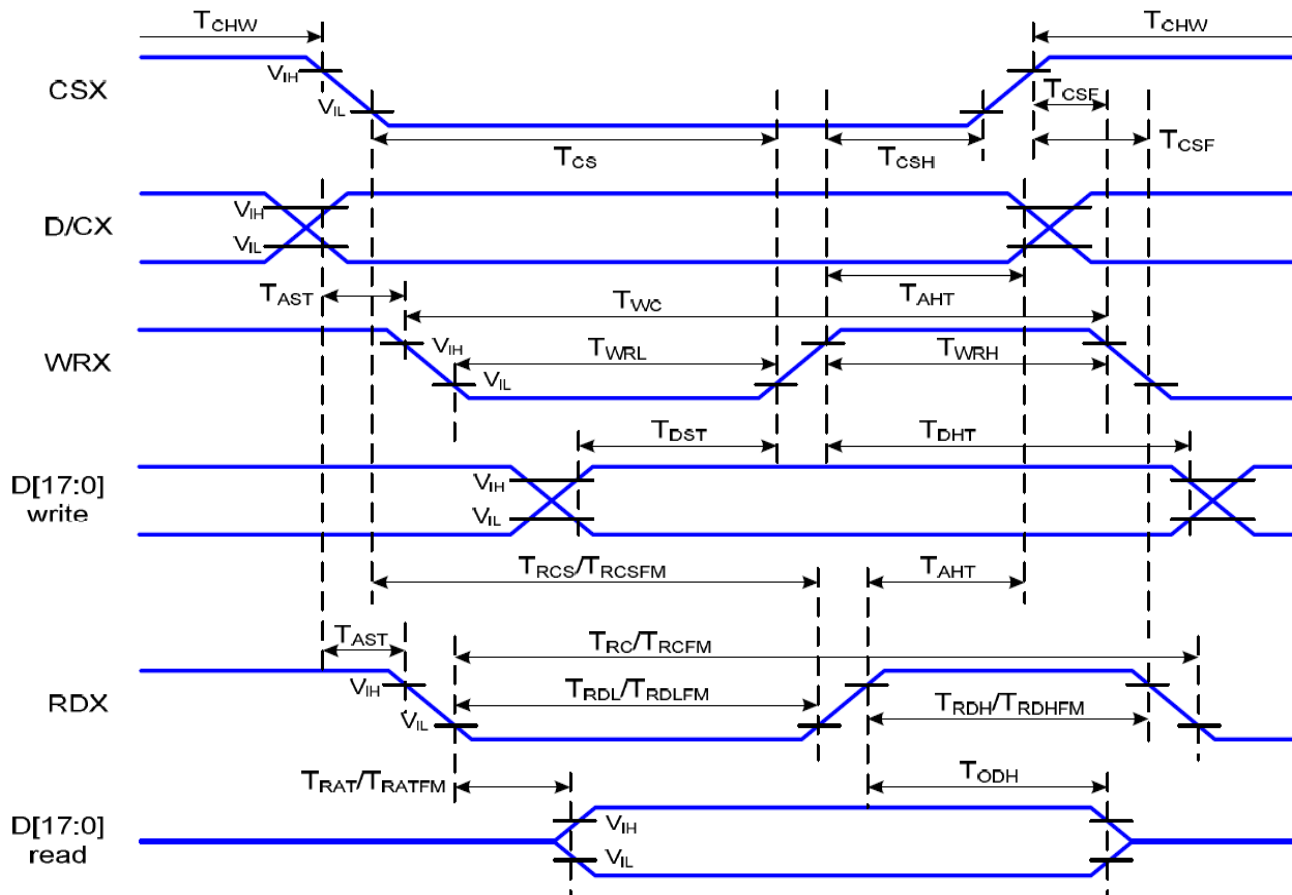


Figure6-1-1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	

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	T_{WRL}	Control pulse “L” duration	15		ns	
RDX(ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX(FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration(FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration(FM)	355		ns	
DB[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table6-1-1 8080 Parallel Interface Characteristics

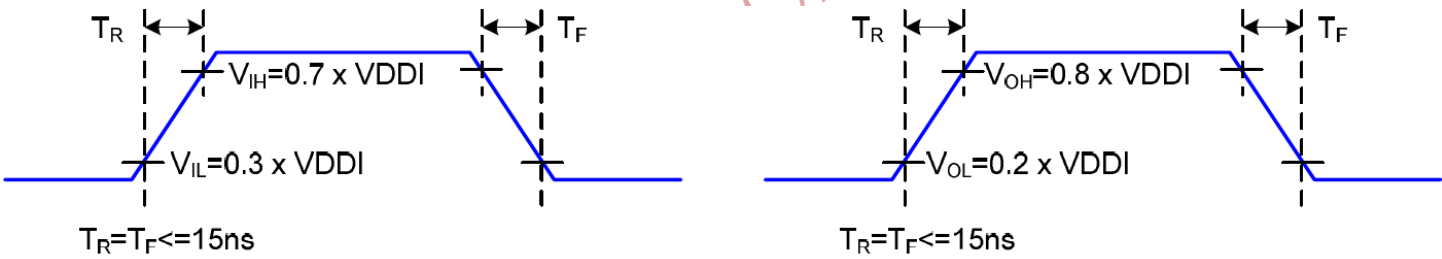


Figure6-1-2 Rising and Falling Timing for I/O Signal

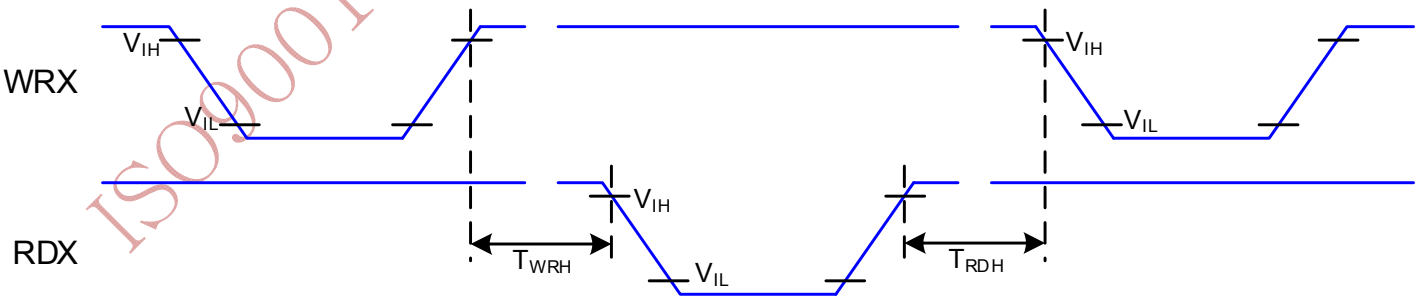


Figure6-1-3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

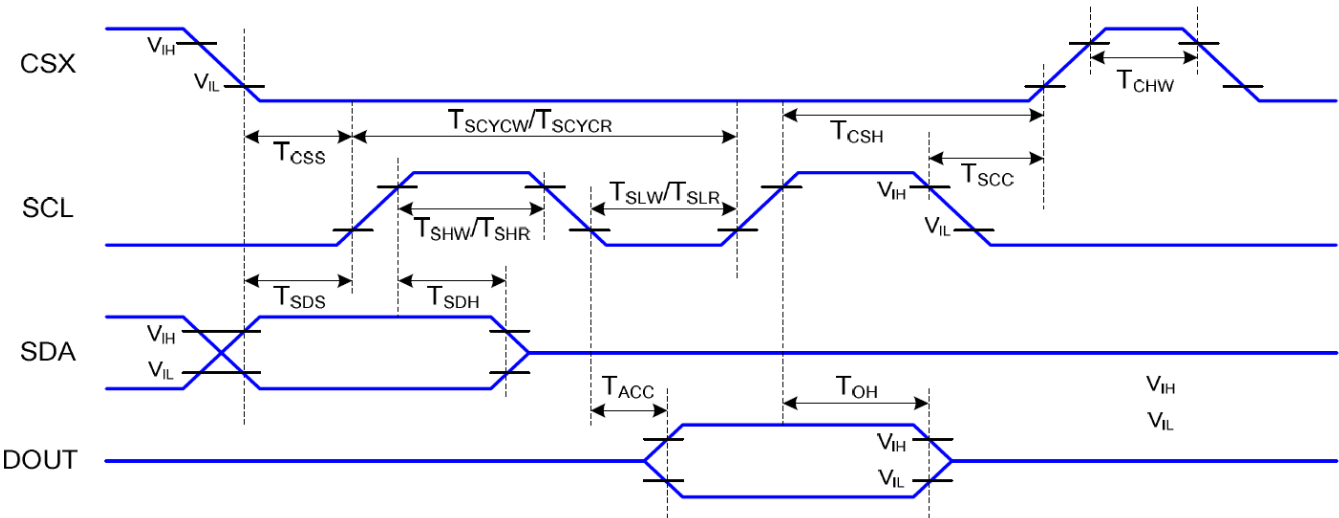


Figure6-2-1 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (Write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table6-2-1 3-line serial Interface Characteristics

Note: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

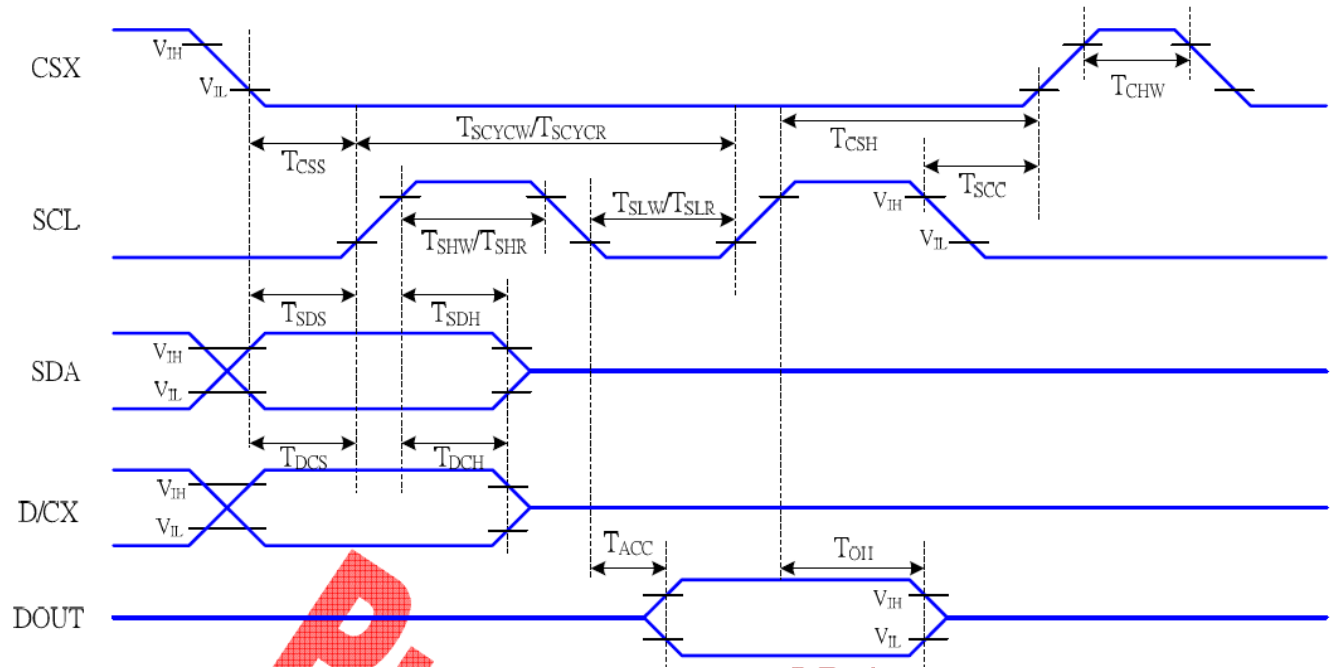


Figure6-3-1 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{CSS}	Chip select setup time (Write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T _{SHW}	SCL "H" pulse width (Write)	15		ns	
	T _{SLW}	SCL "L" pulse width (Write)	15		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T _{DCS}	D/CX setup time	10		Ns	
	T _{DCH}	D/CX hold time	10		ns	
SDA	T _{SDS}	Data setup time	10		ns	



(DIN)	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table6-2-1 4-line serial Interface Characteristics

Note: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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6.4 Parallel RGB Interface Timing Characteristics

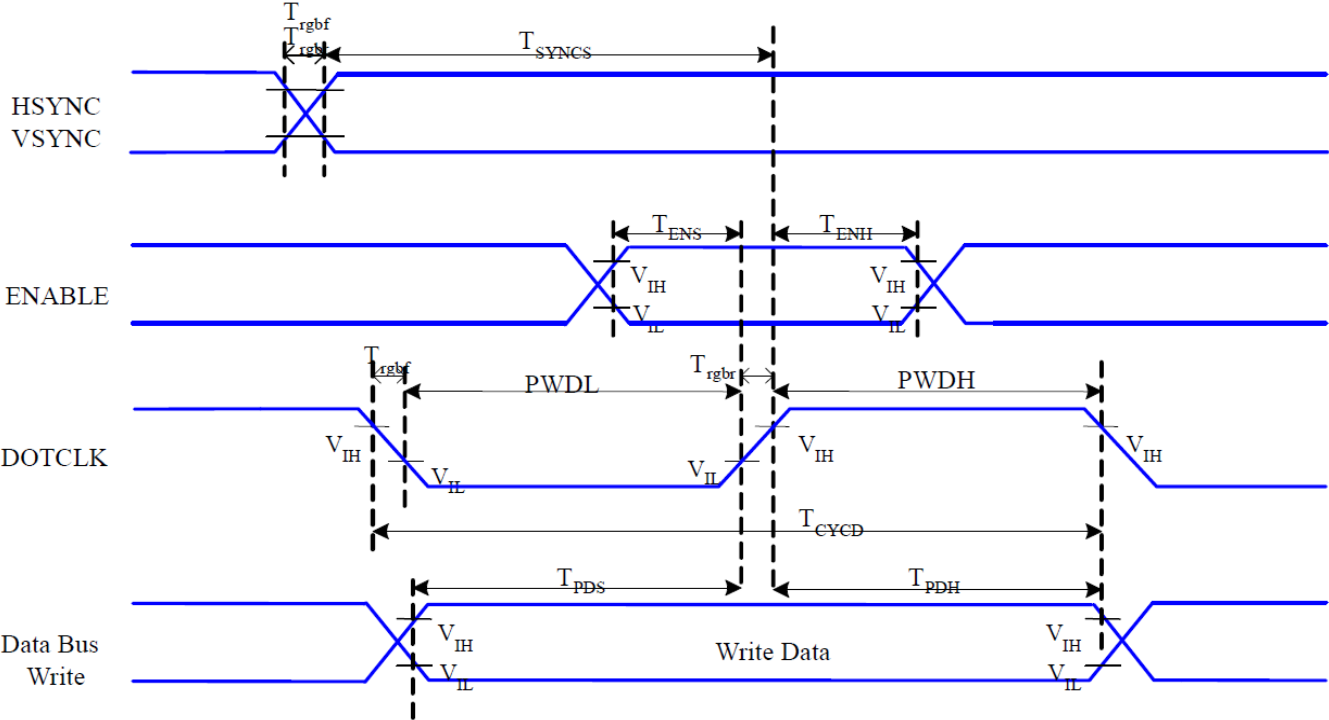


Figure6-4-1 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCs}	VSYNC, HSYNC Setup Time	30		ns	
ENABLE	T_{ENS}	Enable Setup Time	25		ns	
	T_{ENH}	Enable Hold Time	25		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60		ns	
	PWDL	DOTCLK Low-level Pulse Width	60		ns	
	T_{CYCD}	DOTCLK Cycle Time	120		ns	
	T_{rghr} T_{rghf}	DOTCLK Rise/Fall time		20	ns	
DB	T_{PDS}	PD Data Setup Time	50		ns	
	T_{PDH}	PD Data Hold Time	50		ns	

Table6-4-1 18/16 Bits RGB Interface Timing Characteristics



6.5 Reset Timing Characteristics

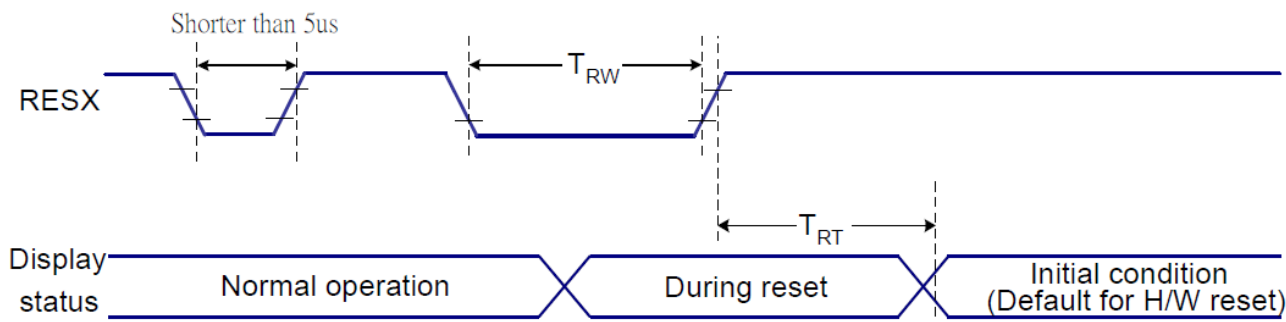


Figure6-5-1 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

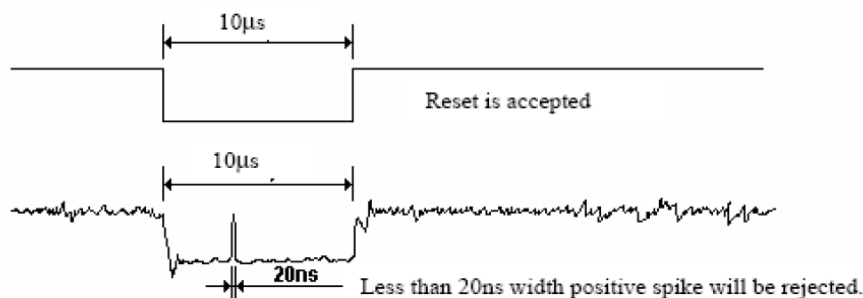
Signal	Symbol	Parameter	Min	Max	Unit
RESX	T_{RW}	Reset pulse duration	10		us
	T_{RT}	Reset cancel		5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



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5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T _{OP}	-20	+70	°C	-
Storage temperature	T _{ST}	-30	+80	°C	-

NOTES:

- If used beyond the absolute maximum ratings, FT6236 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

7.1.2 DC Electrical Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I _{opr}	VDD=2.8V Ta=25°C MCLK= 17.5Mhz	-	4	-	mA	
Monitor mode Current consumption	I _{mon}		-	1.5	-	mA	
Sleep mode Current consumption	I _{slp}			50		uA	
Level input voltage	V _{IH}		0.7V _{DDIO}	-	V _{DDIO}	V	
	V _{IL}		-0.3	-	0.3V _{DDIO}	V	
Level output voltage	V _{OH}	I _{OH} =-0.1mA	0.7V _{DDIO}	-	-	V	
	V _{OL}	I _{OH} =0.1mA	-	-	0.3V _{DDIO}	V	

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常备库存
Standing Stock

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

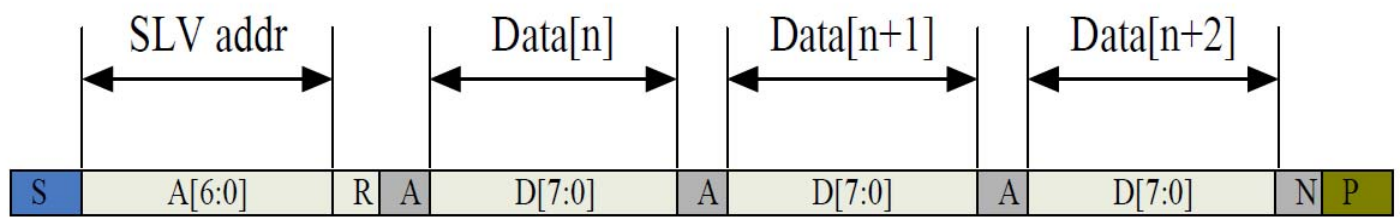


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

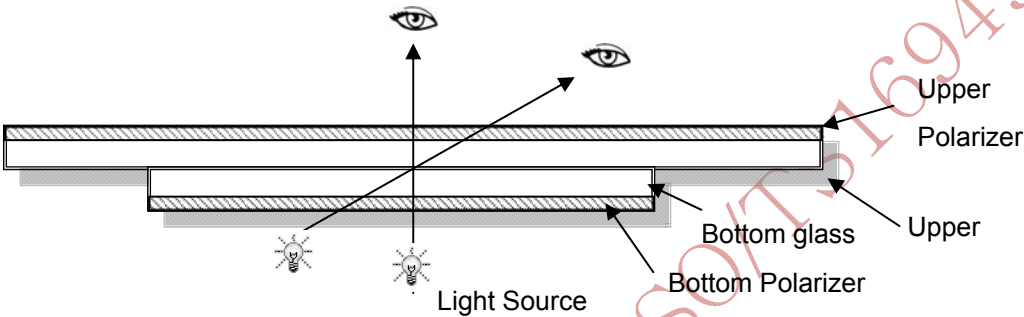
8 LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

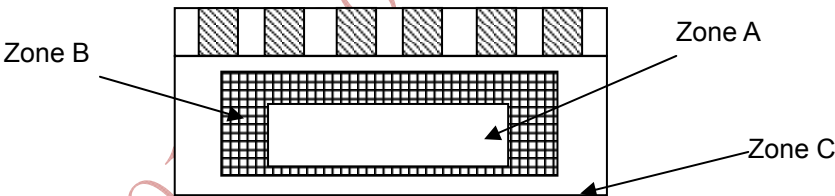
8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



8.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

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常备库存 Standing Stock		长期供货 Long Time supply		品种齐全 In Full Range
		支持小量 NO MOQ		

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

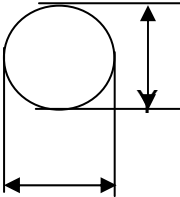
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	



8.1.4 Criteria (Visual)

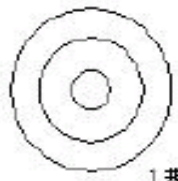
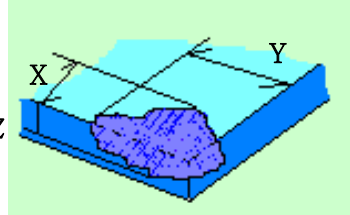
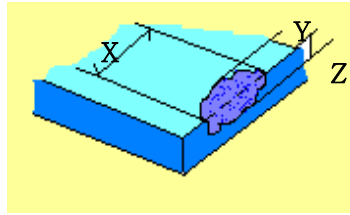
Number	Items	Criteria(mm)
1.0 LCD Crack/Broken <		

Number	Items	Criteria (mm)																													
2.0	Spot defect  X Φ=(X+Y)/2	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)																													
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Accep able Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.10</td><td colspan="3">Ignore</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="3">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.25</td><td colspan="3">2</td></tr><tr><td>Φ > 0.25</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Accep able Qty			A	B	C	Φ≤0.10	Ignore			0.10<Φ≤0.20	3(distance ≥ 10mm)			0.20<Φ≤0.25	2			Φ > 0.25	0								
		Zone Size (mm)		Accep able Qty																											
			A	B	C																										
		Φ≤0.10	Ignore																												
		0.10<Φ≤0.20	3(distance ≥ 10mm)																												
		0.20<Φ≤0.25	2																												
		Φ > 0.25	0																												
		②Dim spot (LCD/TP/Polarizer dim dot, light leakage、 dark spot)																													
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.1</td><td colspan="3">Ignore</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="3">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.30</td><td colspan="3">2</td></tr><tr><td>Φ > 0.30</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.1	Ignore			0.10<Φ≤0.20	3(distance ≥ 10mm)			0.20<Φ≤0.30	2			Φ > 0.30	0								
		Zone Size (mm)		Acceptable Qty																											
			A	B	C																										
		Φ≤0.1	Ignore																												
		0.10<Φ≤0.20	3(distance ≥ 10mm)																												
		0.20<Φ≤0.30	2																												
		Φ > 0.30	0																												
	③ Polarizer accidented spot																														
	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.2</td><td colspan="3">Ignore</td></tr><tr><td>0.3<Φ≤0.5</td><td colspan="3">2(distance ≥ 10mm)</td></tr><tr><td>Φ>0.5</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.2	Ignore			0.3<Φ≤0.5	2(distance ≥ 10mm)			Φ>0.5	0													
	Zone Size (mm)		Acceptable Qty																												
		A	B	C																											
	Φ≤0.2	Ignore																													
0.3<Φ≤0.5	2(distance ≥ 10mm)																														
Φ>0.5	0																														
Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.03</td><td>Igno e</td><td colspan="3">Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr><tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="3">N≤2</td></tr><tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr></table>			Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.03	Igno e	Ignore			0.03<W≤0.05	L≤3.0	N≤2			0.05<W≤0.08	L≤2.0	N≤2			0.08<W	Define as spot defect			
	Width(mm)	Length(mm)	Acceptable Qty																												
			A	B	C																										
	Φ≤0.03	Igno e	Ignore																												
	0.03<W≤0.05	L≤3.0	N≤2																												
	0.05<W≤0.08	L≤2.0	N≤2																												
0.08<W	Define as spot defect																														



3.0	Polarizer Bubble	<table><tr><td rowspan="2"> Zone Size (mm) </td><td colspan="3">Acceptable Qty</td></tr><tr><td>A</td><td>B</td><td>C</td></tr><tr><td>$\Phi \leq 0.2$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.2 < \Phi \leq 0.4$</td><td colspan="2">3(distance ≥ 10 m)</td></tr><tr><td>$0.4 < \Phi \leq 0.6$</td><td colspan="2">2</td></tr><tr><td>$0.6 < \Phi$</td><td colspan="2">0</td></tr></table>				Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore		Ignore	$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 m)		$0.4 < \Phi \leq 0.6$	2		$0.6 < \Phi$	0	
		Zone Size (mm)	Acceptable Qty																						
			A	B	C																				
		$\Phi \leq 0.2$	Ignore		Ignore																				
		$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 m)																						
		$0.4 < \Phi \leq 0.6$	2																						
		$0.6 < \Phi$	0																						
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																							

		TP bubble/ accidented spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="3">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.25$</td><td colspan="3">3 (distance $\geq$</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td colspan="3">2</td></tr><tr><td>$0.3 < \Phi$</td><td colspan="3">0</td></tr></table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore			$0.1 < \Phi \leq 0.25$	3 (distance $\geq$			$0.25 < \Phi \leq 0.3$	2			$0.3 < \Phi$	0		
Size Φ (mm)	Acceptable Qty																											
	A		B	C																								
$\Phi \leq 0.1$	Ignore																											
$0.1 < \Phi \leq 0.25$	3 (distance $\geq$																											
$0.25 < \Phi \leq 0.3$	2																											
$0.3 < \Phi$	0																											
		Assembly deflection	beyond the edge of backlight $\leq 0.15\text{mm}$																									

5.0	TP Related	Newton Ring Newton Ring area>1/3 TP area NG Newton Ring area≤1/3 TP area OK	 1 规律性  2 非规律性  似牛顿环						
		TP corner broken X : length Y : width Z : height <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thicknes</td></tr></table> Circuitry broken is not allowed.	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thicknes	
X	Y	Z							
X≤3.0mm	Y≤3.0mm	Z<LCD thicknes							
		TP edge broken X : length Y : width Z : height <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thicknes	
X	Y	Z							
X≤6.0mm	Y≤2.0mm	Z<LCD thicknes							

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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常备库存
Standing Stock

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	-30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω, ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

Part. No	KD024C-4-C003A	REV	V1.0	Page 32 of 34
常备库存 Standing Stock		长期供货 Long Time supply		品种齐全 In Full Range

支持小量
NO MOQ

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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常备库存
Standing Stock

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range



11. Packing

----TBD-----

ISO9001 : 2008 ISO/TS16949 : 2009

Part. No	KD024C-4-C003A	REV	V1.0	Page 34 of 34
	常 备 库 存 Standing Stock	长 期 供 货 Long Time supply	支持小量 NO MOQ	品 种 齐 全 In Full Range