



**SPECIFICATION
FOR
LCD Module
KD024FM-1B**

MODULE:	KD024FM-1B
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2014.07.20

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		



Revision History

[illegible]

Part. No	KD024FM-1B	REV	V1.0	Page 2 of 30
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General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.4”TFT-LCD contains 240x320 pixels, and can display up to 65K/262K colors.

* Features

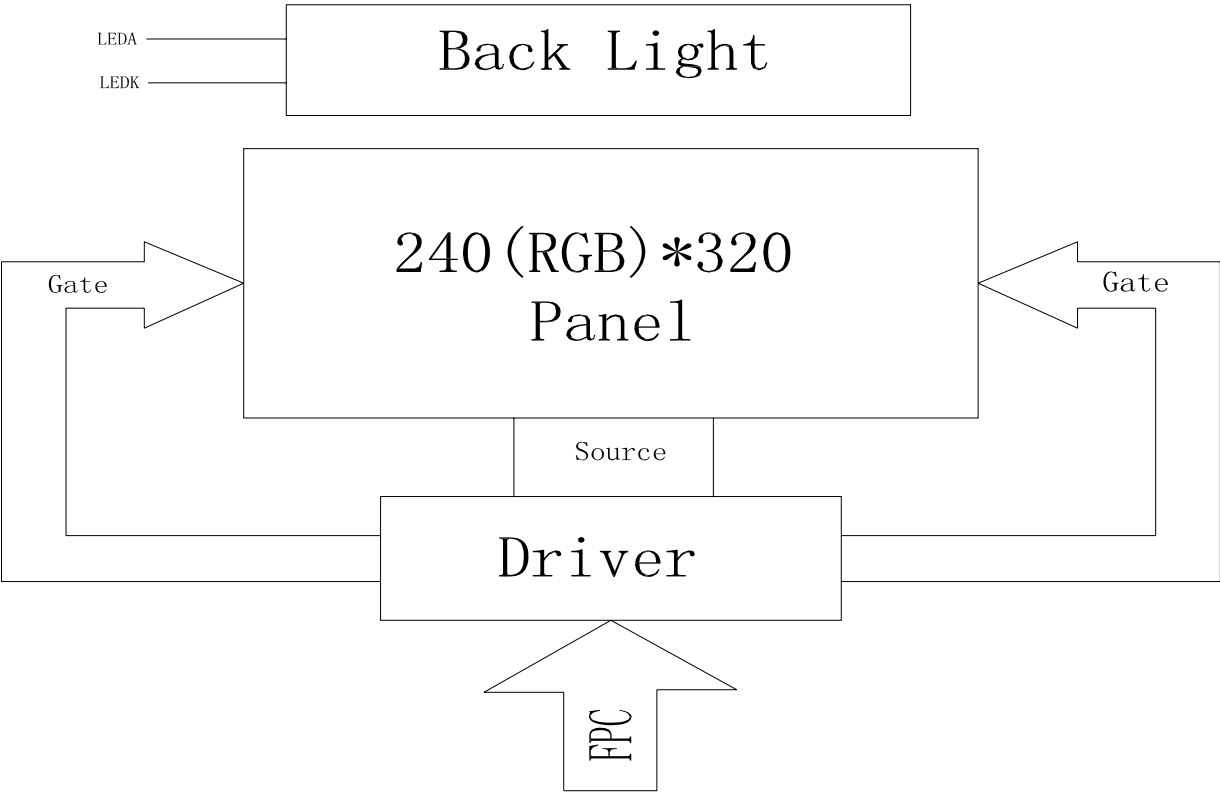
- Input Voltage: 3.3V(TYP).
- Display Colors of TFT LCD: 65K/262Kcolors
- Interface: 8/9/16/18-bits MCU interface,1618-bits RGB interface ,3-line/4-line serial interface.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	36. 72(H) *48.96(V) (2. 4inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*320	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.051 (H) x 0.051 (V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ST7789V	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20~+70	℃	-
Storage temperature	-30~+80	℃	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		42.72		mm	-
	Vertical(V)		60.26		mm	-
	Depth(D)		2.1		mm	-
Weight			TBD		g	-

1. Block Diagram



[illegible]

NO.	Pin Name
1	GND
2	VCC
3	VCC
4	IM2
5	IM1
6	IM0
7	RESET
8	CS
9	DC(SPI-SD)
10	WR(SPI-HS)
11	RD
12	VSVC
13	HSVC
14	ENABLE
15	DOTCLK
16	SDA
17	SCL
18	D001
19	D002
20	D003
21	D004
22	D005
23	D006
24	D007
25	D008
26	D009
27	D010
28	D011
29	D012
30	D013
31	D014
32	D015
33	D016
34	D017
35	SIO
36	LEDA
37	LEDB
38	LEDC
39	LEDD
40	LEDE
41	Y000C
42	Y000D
43	X000C
44	X000D
45	GND

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DB1 T ₀ , 8-bit interface	DB7-DB0
0	0	1	DB1 T ₀ , 16-bit interface	DB15-DB0
0	1	0	DB1 T ₀ , 9-bit interface	DB8-DB0
0	1	1	DB1 T ₀ , 18-bit interface	DB17-DB0
1	0	1	3-wire 9 BIT data serial interface	SDA SCL CS
1	1	0	4-wire 8 BIT data serial interface	SDA SCL CS MS

1. If not use PIN, fix to the GND ,10VCC or NC.
2. If use RGB mode must select serial interface

1. DISPLAY TYPE: 2.4", TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: IPS NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. DRIVER IC: ST7789V (COG)

6. OPERATING TEMP: -20°C TO 70°C

STORAGE TEMP: -30°C TO 80°C

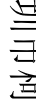
7. BACK LIGHT: LED WHITE, 4 LED, 80mA, 3.2±0.3V

8. ROHS COMPLIANT.

Rev	Revision content description	Date
A	FIRST	2013/03/29

深圳市柯达科电子有限公司

Shenzhen Startek Electronic Technology Co.,Ltd

深圳市柯达科电子科技有限公司 Shenzhen Startek Electronic Technology Co.,Ltd					
TOLERANCE(公差)	DRAWING NAME	KD024FM-1B-LCM			
TOLERANCE UNLESS SPECIFIED	Drawn		Unit		
X.X±0.3	Checked		mm		
X.XX±0.2					
Scale 1:1		Approve		Page 1/1	



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VCI	Supply voltage(3.3V).	P
3	VCI	Supply voltage(3.3V).	P
4	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.	I
5	IM1		I
6	IM0		I
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
9	DC(SPI_SCL)	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.	I
10	WR(SPI_RS,SDA 2)	The data is applied on the rising edge of the SCL signal. If not used, Second Data lane in 2 data lane serial interface. fix this pin at VCI or GND when not in use.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I
12	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
13	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
14	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
15	DOTCLK	Dot clock signal for RGB interface operation.	I



		Fix this pin at VCI or GND when not in use.	
16	SDA1	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
17-34	DB0-DB17	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
35	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
36	LEDA	Anode pin of backlight	P
37	LEDK1	Cathode pin OF backlight	P
38	LEDK2	Cathode pin OF backlight	P
39	LEDK3	Cathode pin OF backlight	P
40	LEDK4	Cathode pin OF backlight	P
41	XR(NC)	Touch panel Right Glass Terminal	A/D
42	YD(NC)	Touch panel Bottom Film Terminal	A/D
43	XL(NC)	Touch panel LIFT Glass Terminal	A/D
44	YU(NC)	Touch panel Top Film Terminal	A/D
45	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	4.65	—	%	Measuring with Polarizer , Reference Only
Transmittance (without Polarizer)		T (%)		—	14.6	—	%	
Contrast		CR		640	800	—	—	(1)(2)
Response time	Rising	T _R		—	16	21	msec	(1)(3)
	Falling	T _F		—	19	24		
Color gamut	(%)			—	70	—	%	C-light
Color chromaticity (CIE1931)	White	W _x		0.290	0.310	0.330	—	(1)(4) CF glass
		W _y		0.316	0.336	0.356		
	Red	R _x		0.627	0.647	0.667	—	
		R _Y		0.297	0.317	0.337	—	
	Green	G _x	0.255	0.275	0.295	—		
		G _Y	0.562	0.582	0.602			
	Blue	B _x	0.120	0.140	0.160	—		
		B _Y	0.068	0.088	0.108			
Viewing angle	Hor.	Θ _L	CR>10	—	80	—	—	(1)(4) Measuring with Polarizer , Reference Only
		Θ _R		—	80	—		
	Ver.	Θ _U		—	80	—		
		Θ _D		—	80	—		
Optima View Direction		Free						(5)

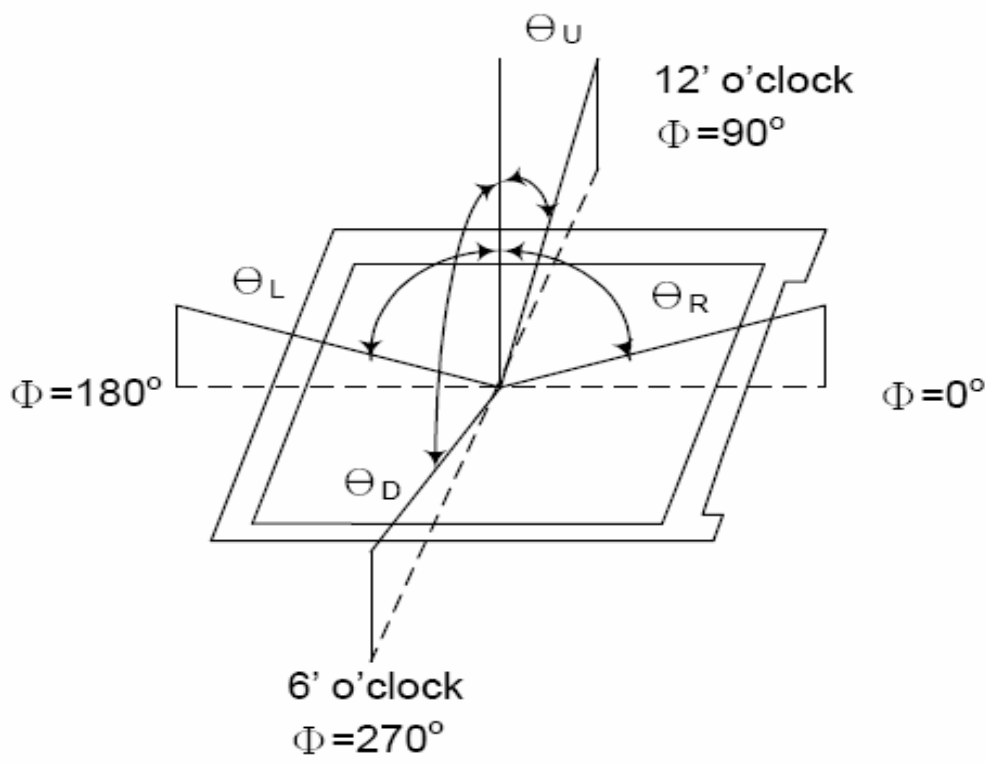
4.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25\pm2^{\circ}\text{C}$
- 15min. warm-up time

4.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

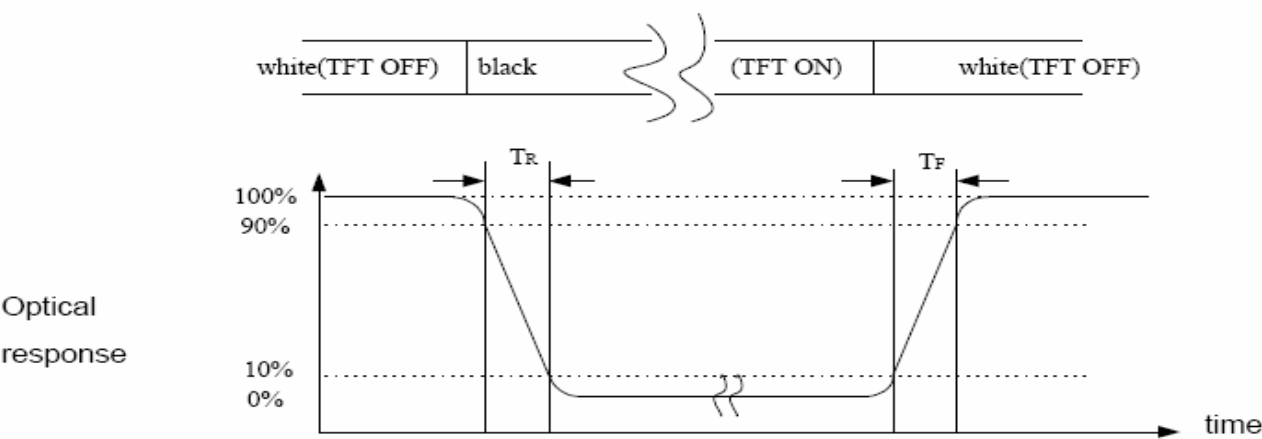
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

Luminance with all pixels white

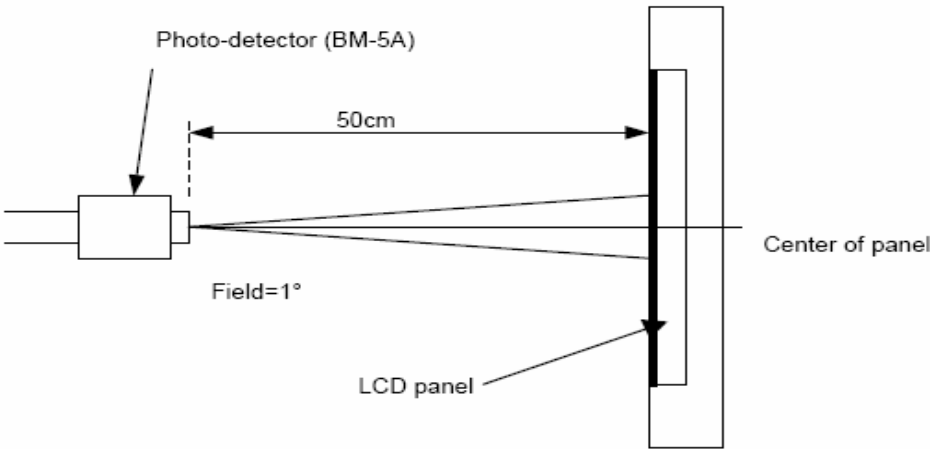
CR =

Luminance with all pixels black

Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

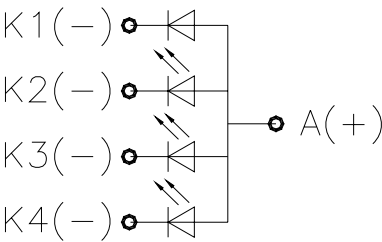
5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.6	3..3	4.2	V	
Digital interface supply Voltage	VDDIO	1.65	1.8	4.2	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V _{IH}	0.7V _{DDIO}		VDDIO	V	
	V _{IL}	GND		0.3V _{DDIO}	V	
Level output voltage	V _{OH}	0.8VDDIO		VDDIO	V	
	V _{OL}	GND		0.2VDDIO	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 chips White LED

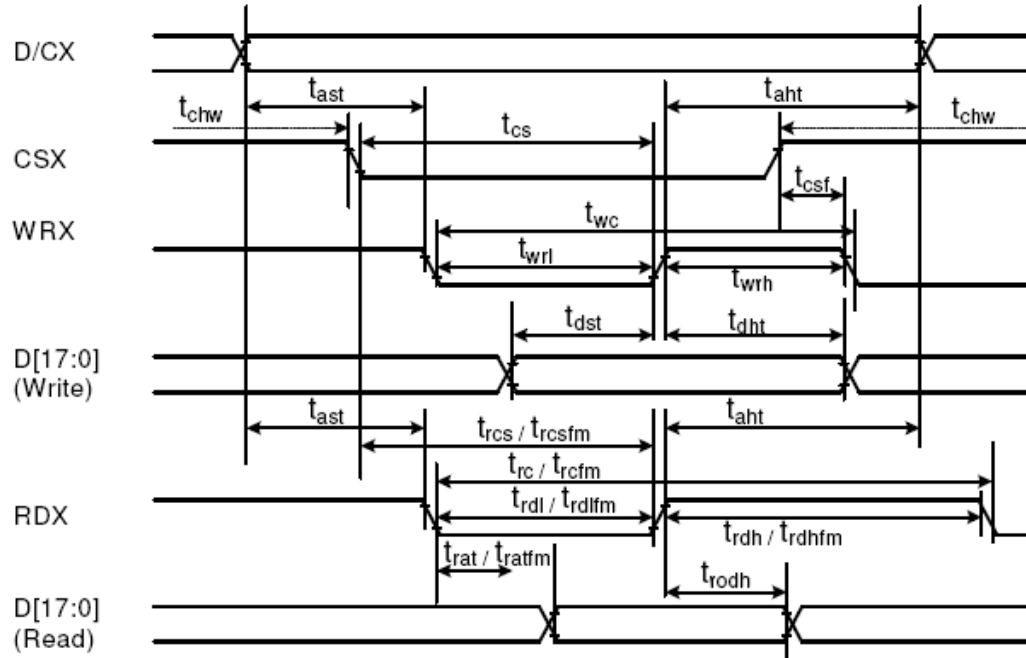
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	60	80	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	450	--	--	cd/m2	IF=80mA
Uniformity	AVg	80	--	--	%	



BLU CIRCUIT DIAGRAM

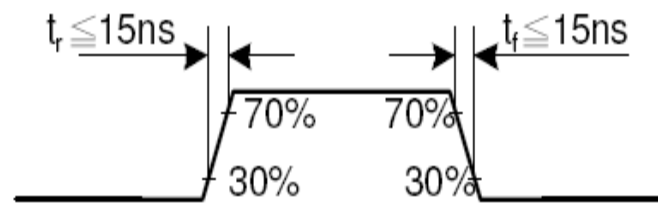
6. AC Characteristic

6.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

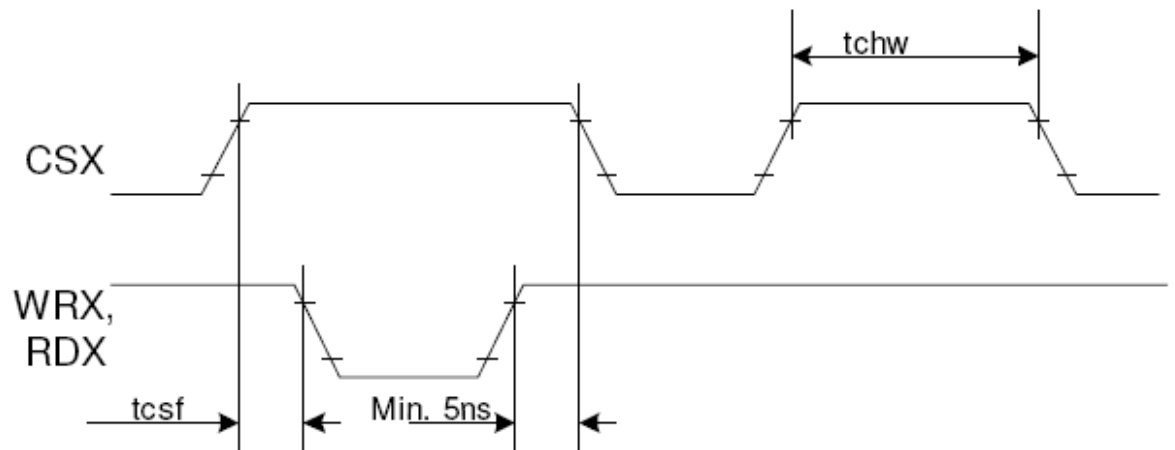


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ahh}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rodh}	Read output disable time	20	80	ns	

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{CI}=2.5\text{V}$ to 3.3V , $V_{SS}=0\text{V}$

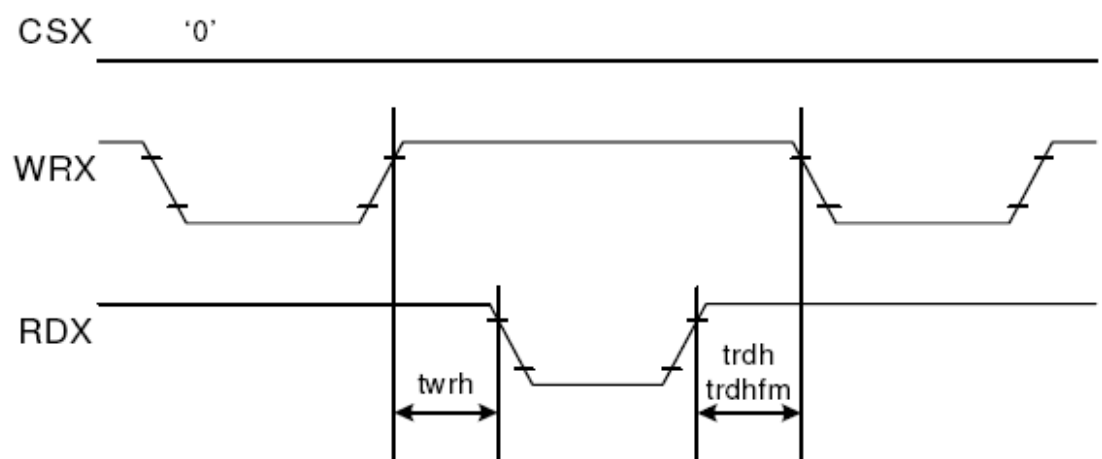


CSX timings :



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

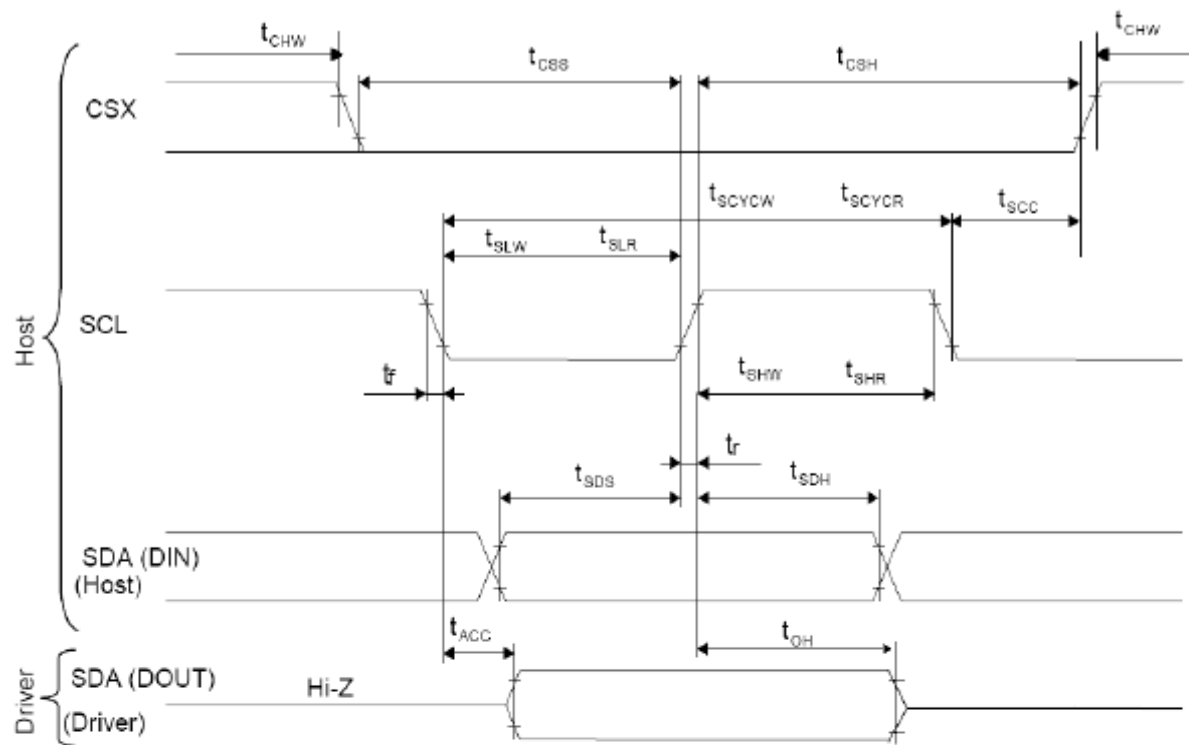
Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

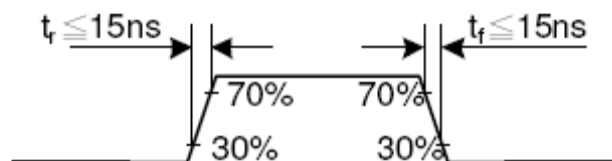


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

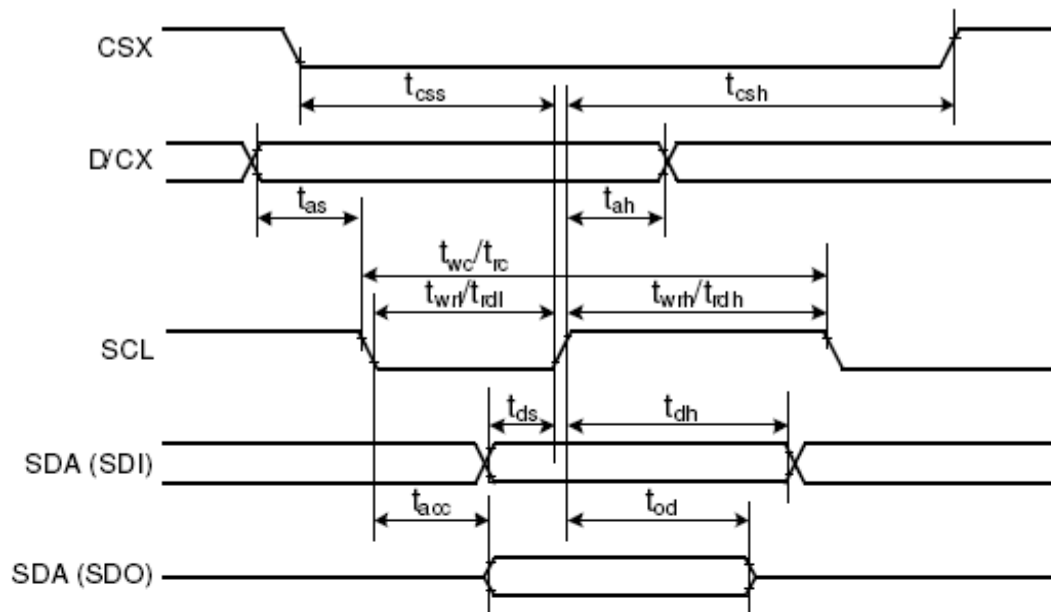


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tc	CSX-SCL Time	60	-	ns	
	ts		65	-	ns	

Note: $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

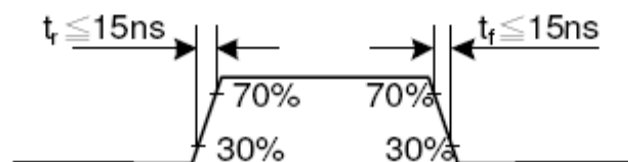


6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

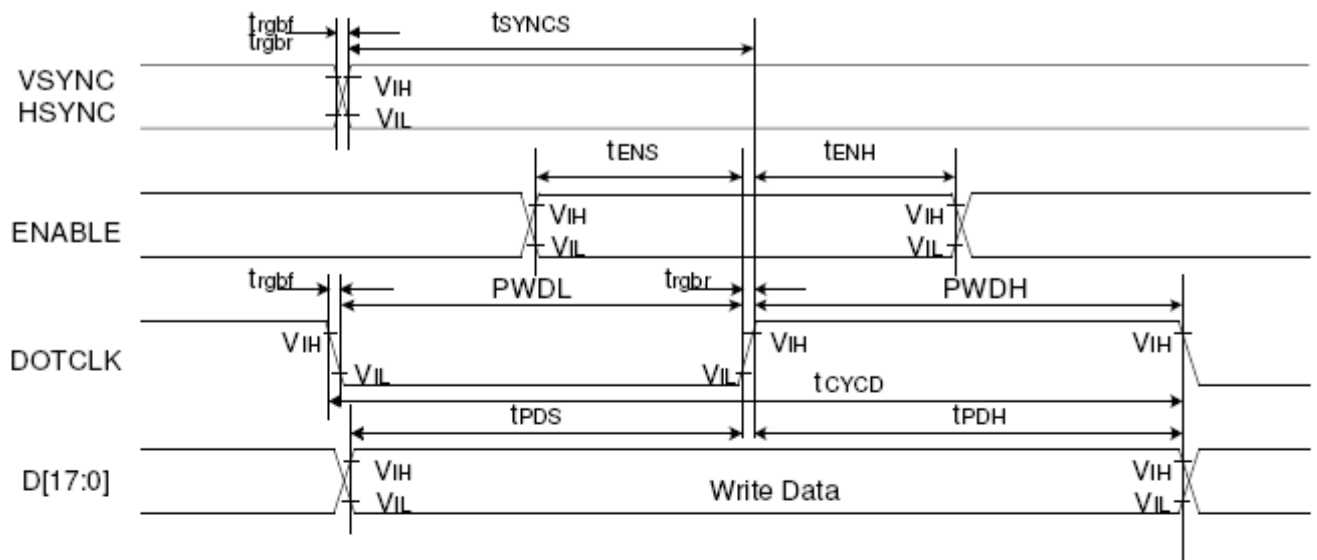


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Read)	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	40	-	ns	
	t_{wrl}	SCL "L" pulse width (Write)	40	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{rdl}	SCL "L" pulse width (Read)	60	-	ns	
	t_{as}	D/CX setup time	10	-		
D/CX	t_{ah}	D/CX hold time (Write / Read)	10	-		
	t_{ds}	Data setup time (Write)	30	-	ns	
SDA / SDI (Input)	t_{dh}	Data hold time (Write)	30	-	ns	
	t_{acc}	Access time (Read)	10	-	ns	For maximum $C_L=30pF$
SDA / SDO (Output)	t_{od}	Output disable time (Read)	10	50	ns	For minimum $C_L=8pF$

Note: $T_a = 25^\circ C$, $V_{DDI}=1.65V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $AGND=VSS=0V$

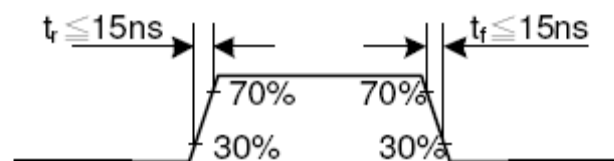


6.4 Parallel RGB Interface Timing Characteristics

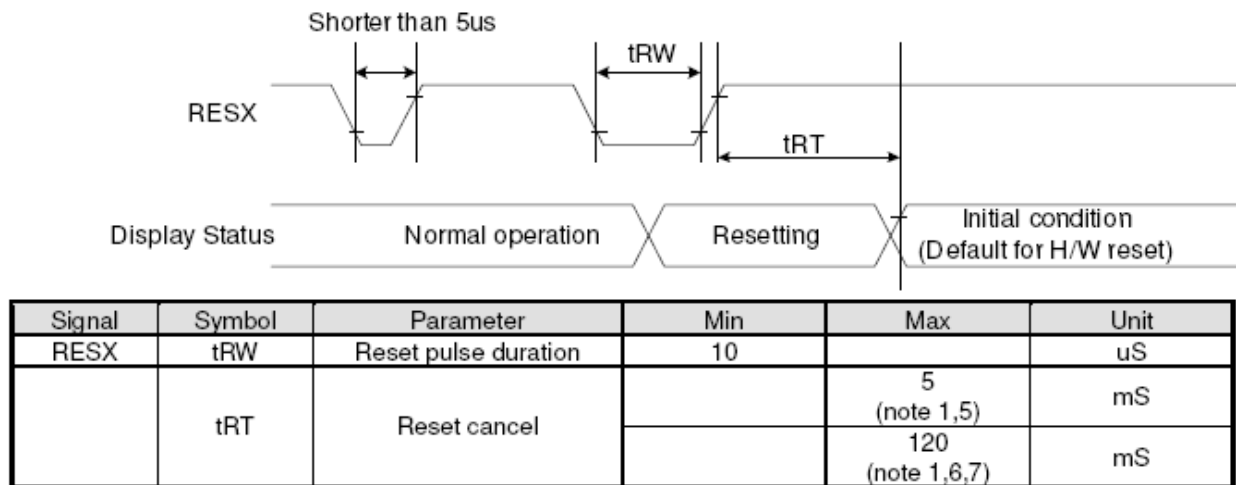


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	$PWDH$	DOTCLK high-level period	15	-	ns	
	$PWDL$	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbr}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	$PWDH$	DOTCLK high-level pulse period	15	-	ns	
	$PWDL$	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbr}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI} = 1.65V$ to $3.3V$, $V_{CI} = 2.5V$ to $3.3V$, $AGND = VSS = 0V$



6.5 Reset Timing Characteristics



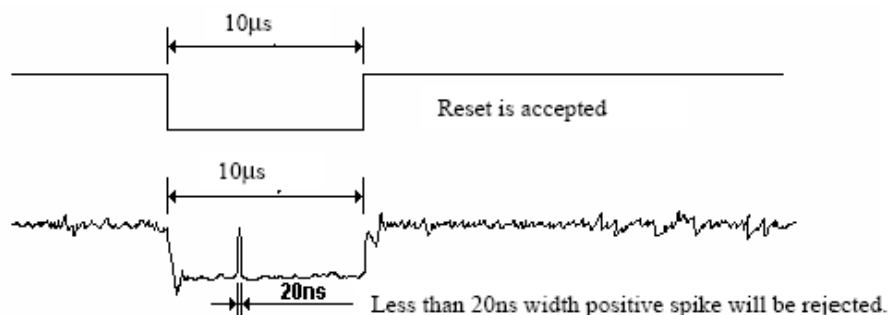
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out

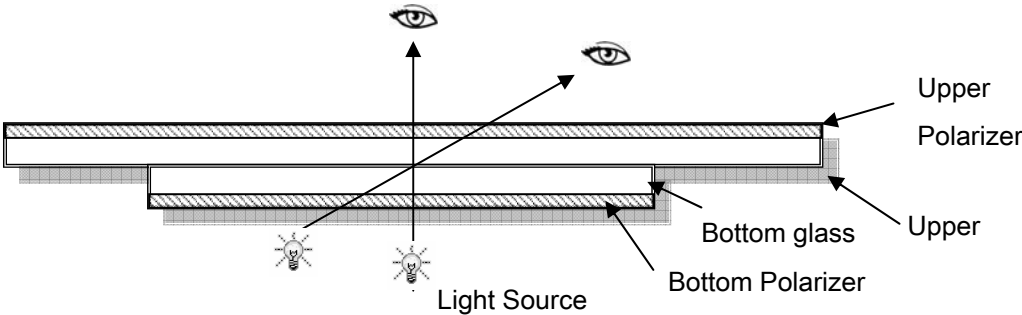
7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

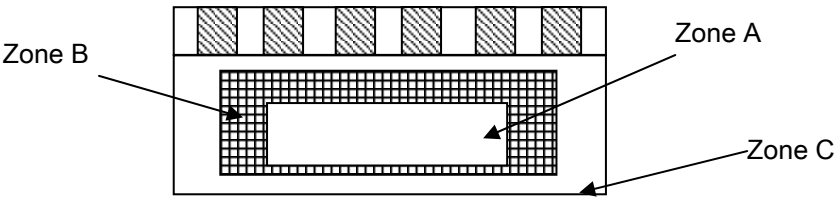
7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30–50cm



7.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

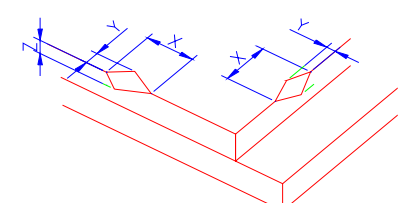
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

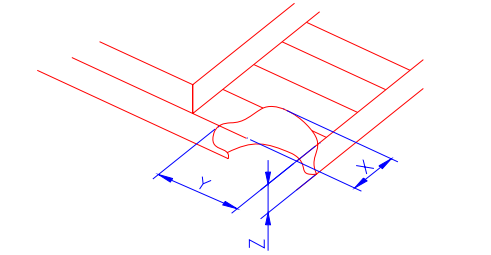
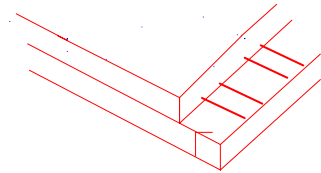
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

7

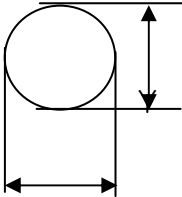
7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken	(1) The edge of LCD broken	 <table> <tr> <th>X</th><th>Y</th><th>Z</th></tr> <tr> <td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
NOTE: X: Length Y: Width								

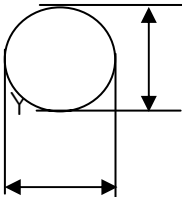


Z: Height L: Length of ITO, T: Height of LCD	(2)LCD corner broken	 <table border="1" data-bbox="922 546 1332 647"><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T
	X	Y	Z					
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							



Number	Items	Criteria (mm)																									
2.0	Spot defect  X Φ=(X+Y)/2	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)																									
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.10<Φ≤0.15</td><td colspan="2">3(distance≥10mm)</td></tr><tr><td>0.15<Φ≤0.2</td><td colspan="2">1</td></tr><tr><td>0.2<Φ</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.10	Ignore		Ignore	0.10<Φ≤0.15	3(distance≥10mm)		0.15<Φ≤0.2	1		0.2<Φ	0						
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Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr><tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr><tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr></table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.03	Ignore	Ignore		Ignore	0.03<W≤0.05	L≤3.0	N≤2		0.05<W≤0.08	L≤2.0	N≤2		0.08<W	Define as spot defect			
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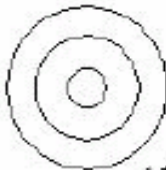
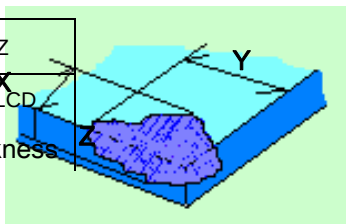
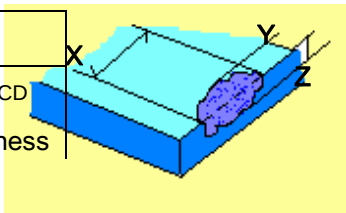


Items	Criteria (mm)																																																																	
Spot defect  X Y $\Phi=(X+Y)/2$	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain) <table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.10$</td><td colspan="3">Ignore</td></tr><tr><td>$0.10<\Phi\leq0.15$</td><td colspan="3">3(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.15<\Phi\leq0.2$</td><td colspan="3">1</td></tr><tr><td>$0.2<\Phi$</td><td colspan="3">0</td></tr></table> ②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot) <table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.1$</td><td colspan="3">Ignore</td></tr><tr><td>$0.1<\Phi\leq0.2$</td><td colspan="3">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.2<\Phi\leq0.3$</td><td colspan="3">1</td></tr><tr><td>$\Phi>0.3$</td><td colspan="3">0</td></tr></table> ③ Polarizer accidented spot <table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.2$</td><td colspan="3">Ignore</td></tr><tr><td>$0.2<\Phi\leq0.5$</td><td colspan="3">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$\Phi>0.5$</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.10$	Ignore			$0.10<\Phi\leq0.15$	3(distance $\geq 10\text{mm}$)			$0.15<\Phi\leq0.2$	1			$0.2<\Phi$	0			Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.1$	Ignore			$0.1<\Phi\leq0.2$	2(distance $\geq 10\text{mm}$)			$0.2<\Phi\leq0.3$	1			$\Phi>0.3$	0			Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.2$	Ignore			$0.2<\Phi\leq0.5$	2(distance $\geq 10\text{mm}$)			$\Phi>0.5$	0		
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	Polarizer Bubble	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.2$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.2 < \Phi \leq 0.4$</td><td colspan="2">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.4 < \Phi \leq 0.6$</td><td colspan="2">1</td></tr><tr><td>$0.6 < \Phi$</td><td colspan="2">0</td></tr></table>				Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore		Ignore	$0.2 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		$0.4 < \Phi \leq 0.6$	1		$0.6 < \Phi$	0							
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$0.6 < \Phi$	0																														
	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																													

		TP bubble/ accidented spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.1</td><td colspan="3">Ignore</td></tr><tr><td>0.1<Φ≤0.2</td><td colspan="3">2</td></tr><tr><td>0.2<Φ≤0.3</td><td colspan="3">1</td></tr><tr><td>0.3<Φ</td><td colspan="3">0</td></tr></table>	Size Φ(mm)	Acceptable Qty			A	B	C	Φ≤0.1	Ignore			0.1<Φ≤0.2	2			0.2<Φ≤0.3	1			0.3<Φ	0		
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	A	B	C																							
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0.1<Φ≤0.2	2																									
0.2<Φ≤0.3	1																									
0.3<Φ	0																									
		Assembly deflection	beyond the edge of backlight ≤0.15mm																							

5.0	TP Related	Newton Ring	Newton area>1/3 TP NG	Ring area	 1.规律性					
			Newton area≤1/3 TP OK	Ring area	 2.非规律性					
					 似牛顿环					
		TP corner broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thickness	
X	Y	Z								
X≤3.0mm	Y≤3.0mm	Z<LCD thickness								
		TP edge broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thickness</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thickness	
X	Y	Z								
X≤6.0mm	Y≤2.0mm	Z<LCD thickness								



Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃, 90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	- 30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10.Packing

