SPECIFICATION
FOR
LCD Module
KD040C-2-TP

MODULE:	**KD040C-2-TP**
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2012.06.08

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Data	Rev. No.	Page	Summary
2012.06.08	V1.0	ALL	FIRST ISSUE

Contents

General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.0TFT-LCD contains 480x800 pixels, and can display up to 65K/262K/16.7M colors.

* Features

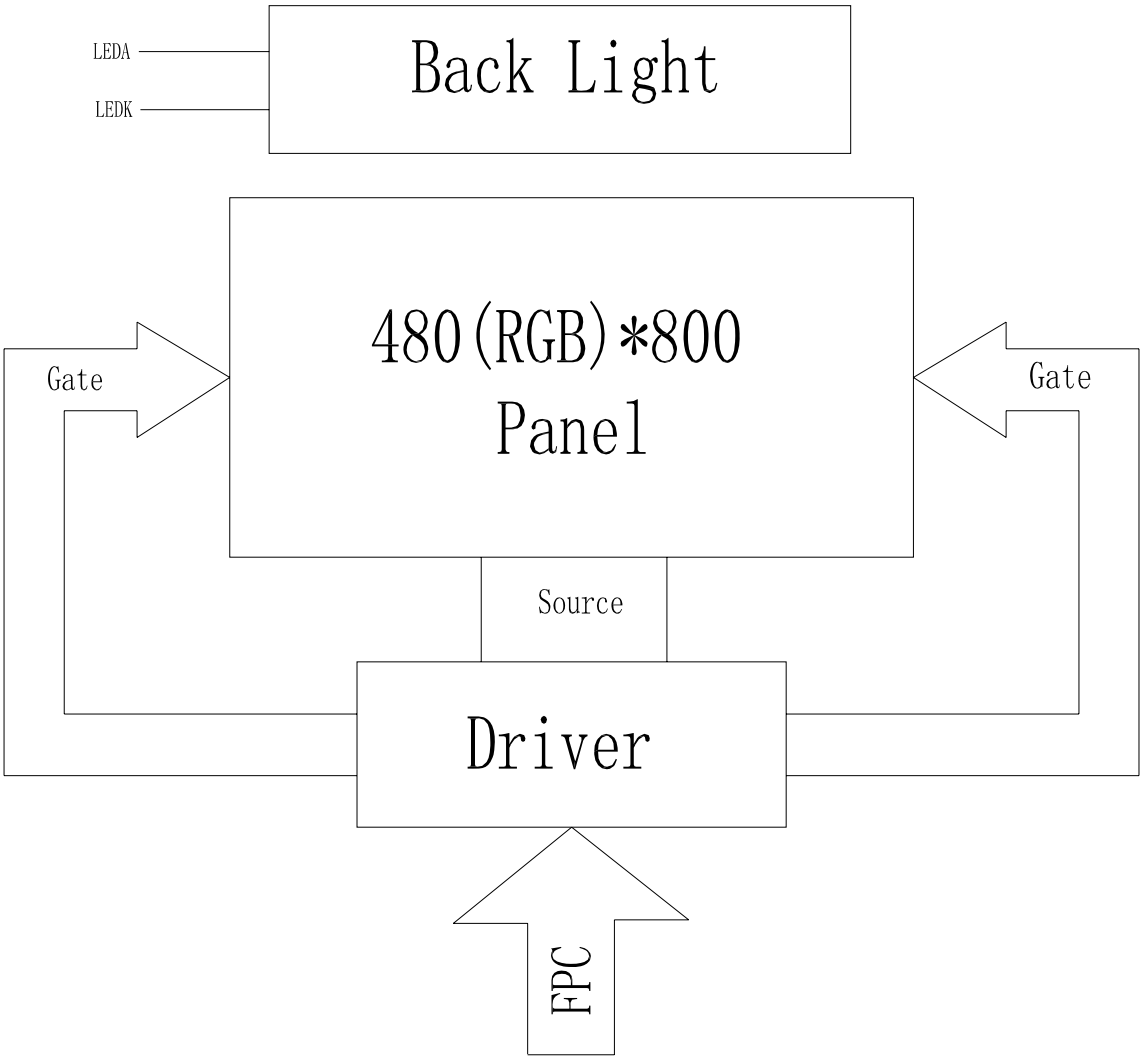
-Low Input Voltage: 3.3V(TYP)
-Display Colors of TFT LCD: 65K/262K/16.7M colors
-RGB Interface: 8BIT/9BIT/16BIT/18BIT/24BIT MCU, 3SPI/4SPI+16BIT/18BIT/24BIT RGB

eral Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	51.84(H)*86.40 (V) (4.0inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*800	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.108(H)*0.108(V)	mm	-
Viewing angle	6:00	o'clock	-
Controller IC	ILI9806	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

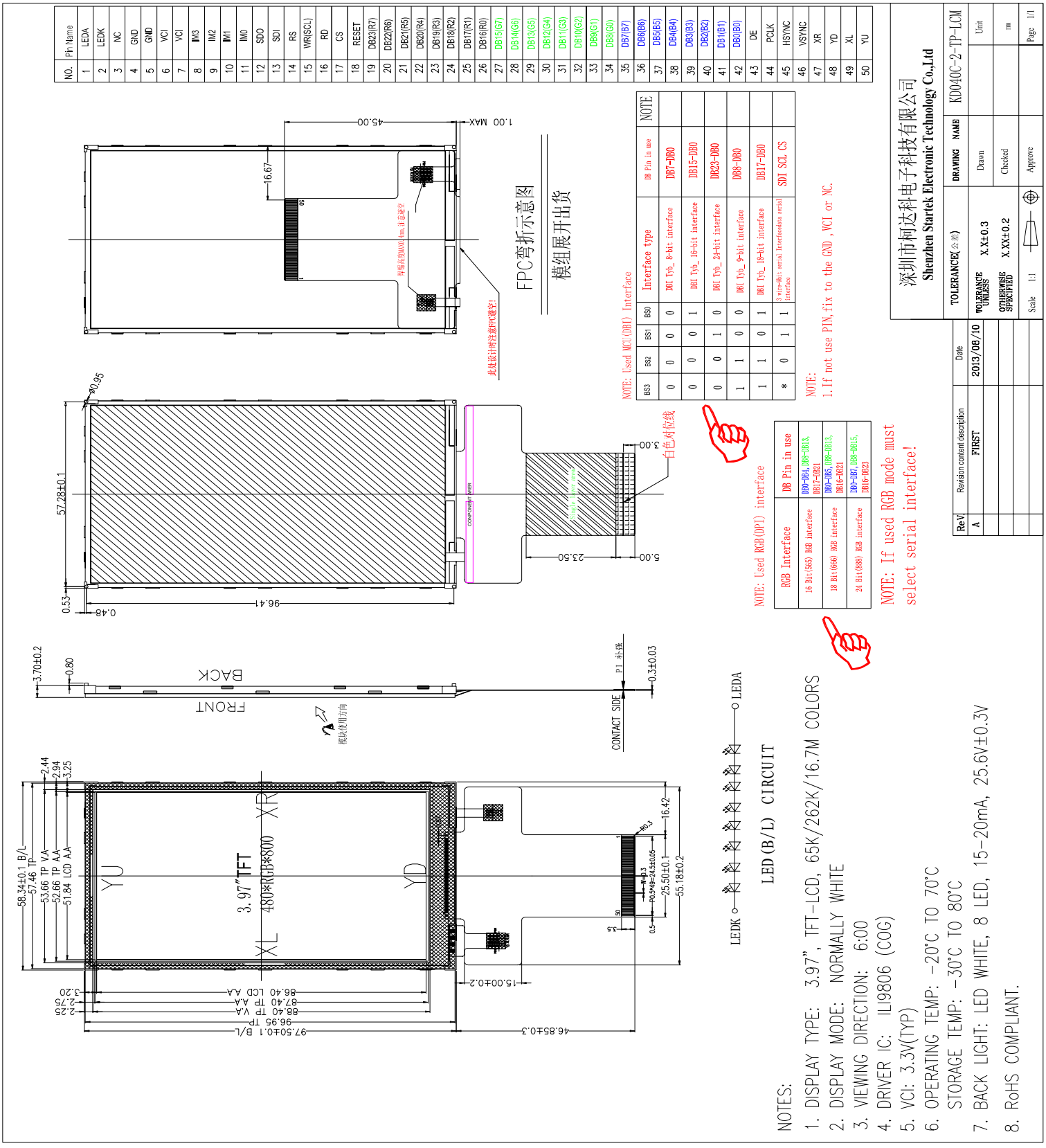
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		58.34		mm	-
	Vertical(V)		97.50		mm	-
	Depth(D)		3.7		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	LEDA	Anode pin of backlight	P
2	LEDK	Cathode pin OF backlight	P
3	NC	NC	
4	GND	Ground.	P
5	GND	Ground.	P
6	VCI	Supply voltage(3.3V).	P
7	VCI	Supply voltage(3.3V).	P
8	IM3	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.	I
9	IM2		I
10	IM1		I
11	IM0		I
12	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
13	SDI	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND	I
14	RS	This pin is used to select “Data or Command” in the parallel interface. When RS = ’1’, data is selected. When RS = ’0’, command is selected.	I
15	WR(SCL)	The data is applied on the rising edge of the SCL signal. fix this pin at VCI or GND when not in use.	I
16	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I
17	CS	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.	I

18	RESET	This signal will reset the device and must b e applied to properly initialize the chip.	I
19-42	DB23-DB0	24-bit parallel bi-directional data bus for M CU system and RGB interface mode . Fix to GND level when not in use	I/O
43	DE	Data enable signal for RGB interface operatio n. fix this pin at VCI or GND when not in use.	
44	PCLK	Dot clock signal for RGB interface operation Fix this pin at VCI or GND when not in use.	I
45	HSYNC	Line synchronizing signal for RGB interface o peration. fix this pin at VCI or GND when not in use	I
46	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
47	XR	Touch panel Right Glass Terminal	A/D
48	YD	Touch panel Bottom Film Terminal	A/D
49	XL	Touch panel LIFT Glass Terminal	A/D
50	YU	Touch panel Top Film Terminal	A/D

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	4.29	—	—	
Transmittance (without Polarizer)		T(%)		—	12.16	—	—	
Contrast		CR		560	700	—		(1)(2)
Response time	Rising	T_R		—	4	8	msec	(1)(3)
	Falling	T_F		—	12	24		
Color gamut	S(%)			—	62	—	%	
Color chromaticity (CIE1931)	White	W_x		0.283	0.303	0.323		(1)(4) CF glass
		W_y		0.305	0.325	0.345		
	Red	R_x		0.606	0.626	0.646		
		R_Y		0.314	0.334	0.354		
	Green	G_x		0.257	0.277	0.297		
		G_Y		0.529	0.549	0.569		
	Blue	B_x		0.122	0.142	0.162		
		B_Y		0.102	0.122	0.142		
Viewing angle	Hor.	Θ_L	CR>10	60	70	—		(1)(4) Viewing Angle base on using EWV Polarizer, Reference Only
		Θ_R		60	70	—		
	Ver.	Θ_U		60	70	—		
		Θ_D		40	60	—		
Optima View Direction		12 O'clock						(5)

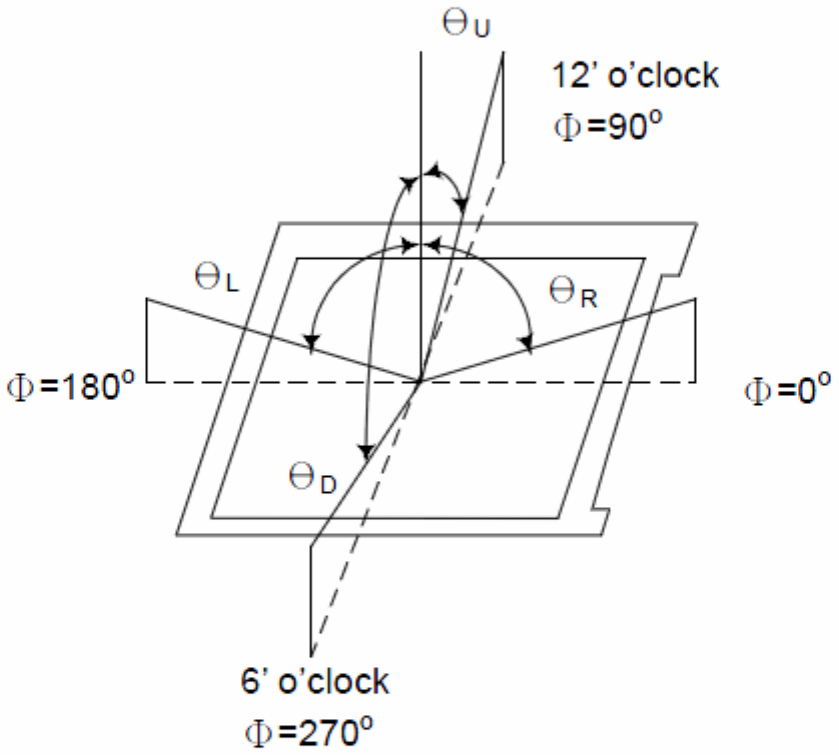
4.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.

4.3 Measuring Equipment

■ FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

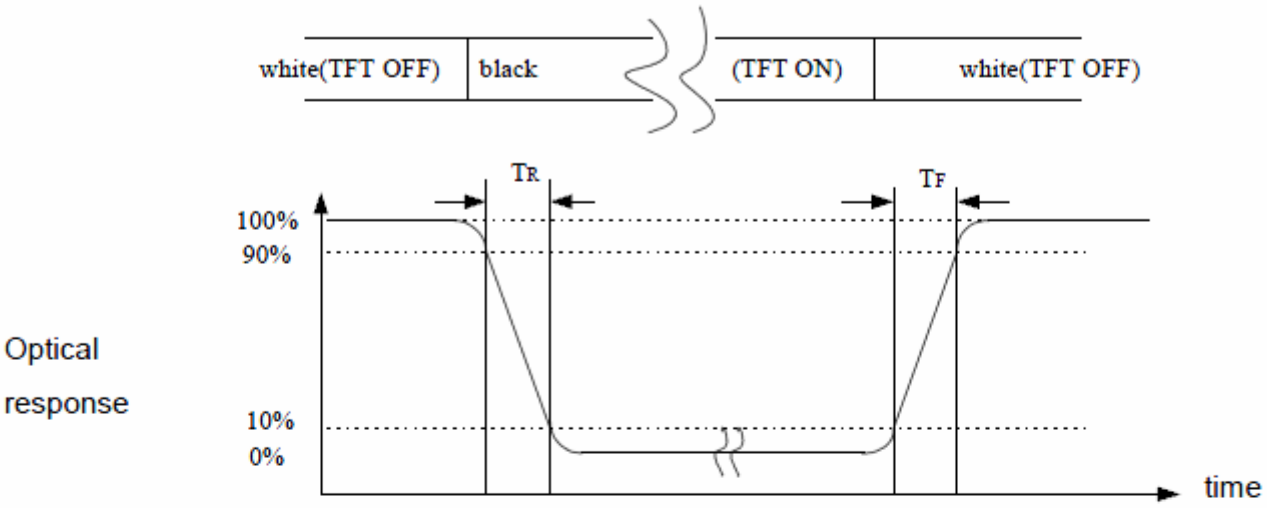
Note (1) Definition of Viewing Angle:



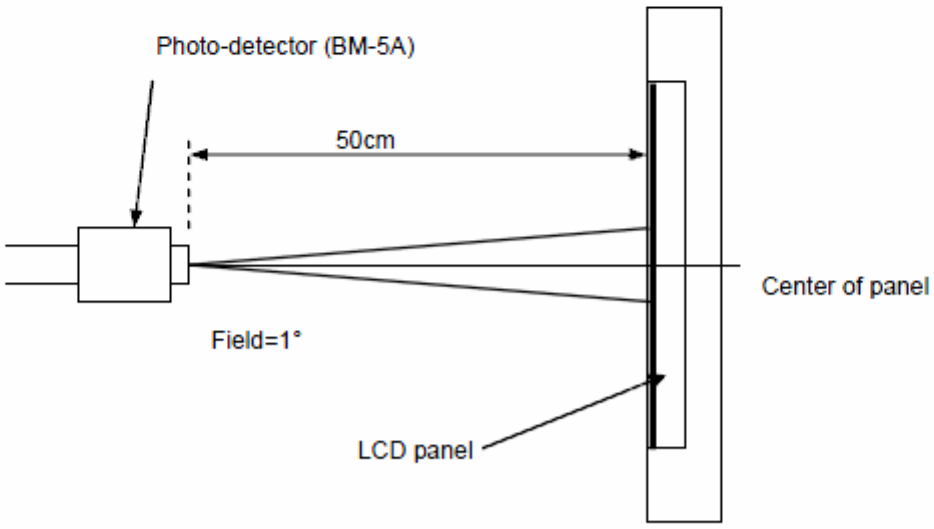
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

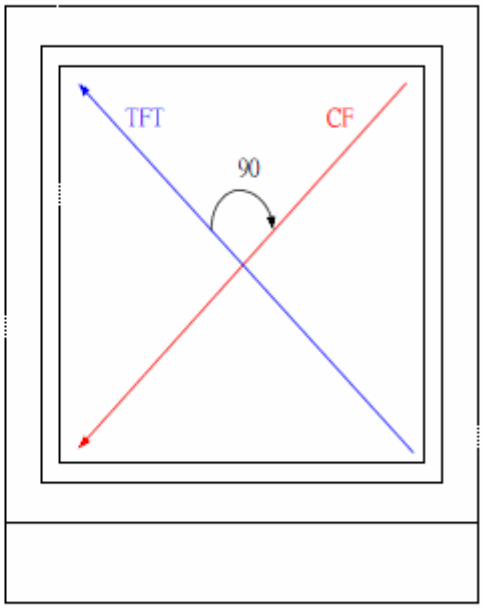
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



TFT Face up

5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	**V**
Digital interface supple Voltage	VDDIO	-0.3	4.6	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.4	3..3	4.2	V	
Digital interface supple Voltage	VDDIO	1.65	3.3	4.2	V	
Normal mode Current consumption	IDD	--	30	--	mA	
Level input voltage	V_{IH}	0.7V_{DDIO}		VDDIO	V	
	V_{IL}	GND		0.3V_{DDIO}	V	
Level output voltage	V_{OH}	0.8VDDIO		VDDIO	V	
	V_{OL}	GND		0.2VDDIO	V	

5.3 LED Backlight Characteristics

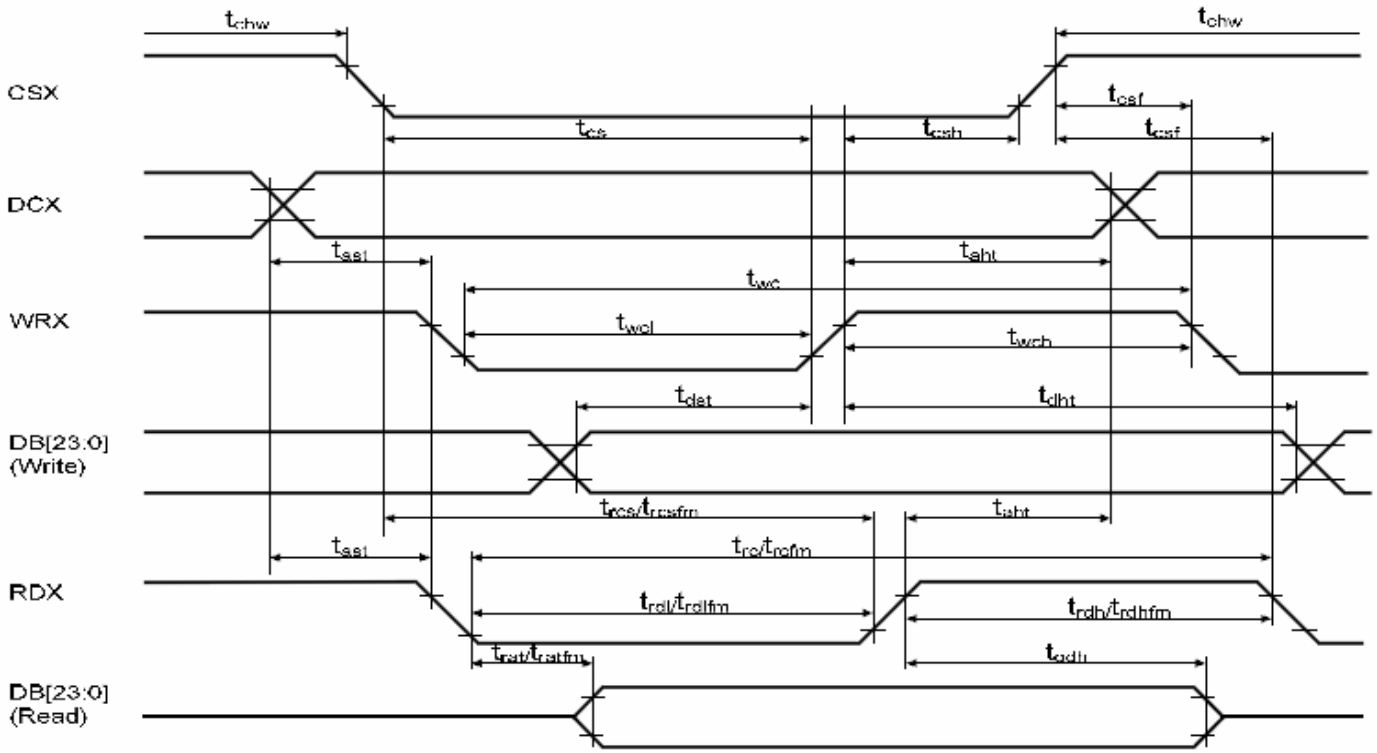
The back-light system is edge-lighting type with 4chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	15	20	--	mA	
Forward Voltage	V_F	--	25.6	--	V	
LCM Luminance	L_V	300	--	--	cd/m2	IF=20mA
Uniformity	AVg	80	--	--	%	

LED(B/L) CIRCUIT

6. AC Characteristic

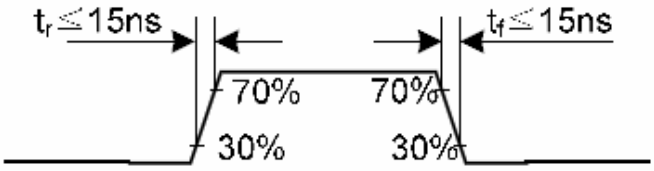
6.1. Display Parallel 24/18/16/9/8-bit Interface Timing Characteristics (8080-system)



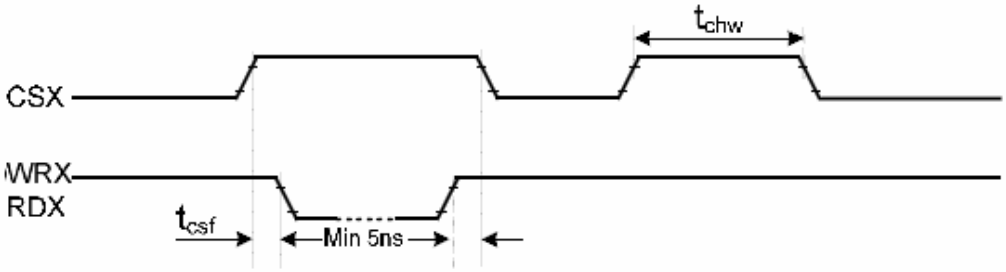
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	10	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	10	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	-
WRX	twc	Write cycle	30	-	ns	-
	twrh	Write Control pulse H duration	10	-	ns	-
	twrl	Write Control pulse L duration	10	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from the Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0], DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	CL = 30pF (maximum) CL = 8pF (minimum)
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trodh	Read output disable time	20	80	ns	

Notes:

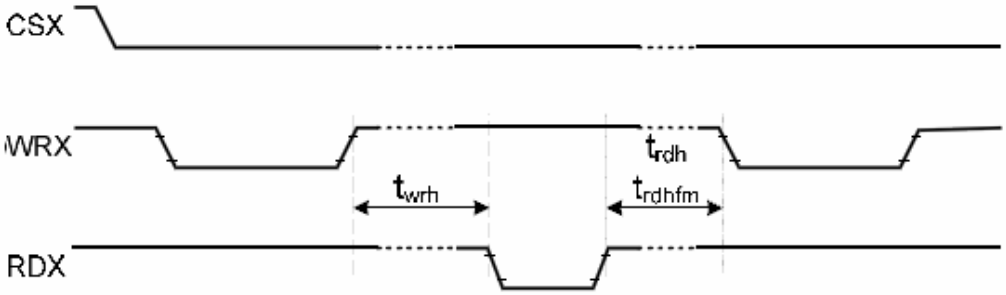
1. Ta = -30 to 70°C, VDDI = 1.65V to 3.3V, VDDA = 2.6V to 4.8V, VSSAM = GND= 0V
2. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.
3. Input signal rising and falling time:



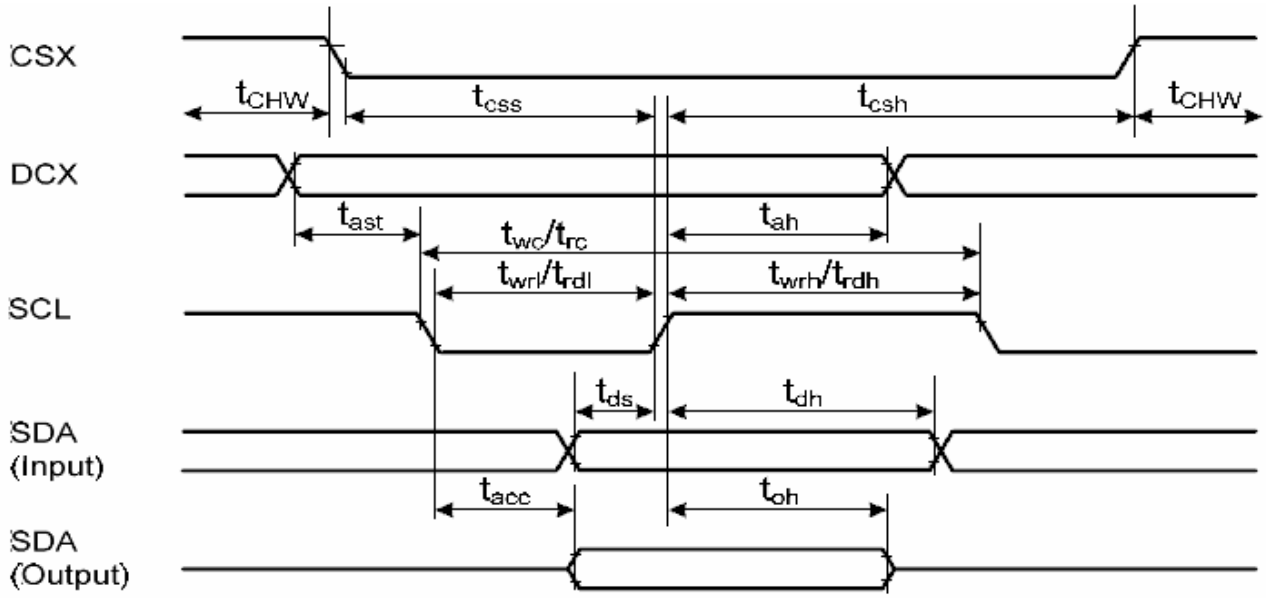
4. The CSX timing:



5. The Write-to-Read or the Read-to-Write timing:



6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

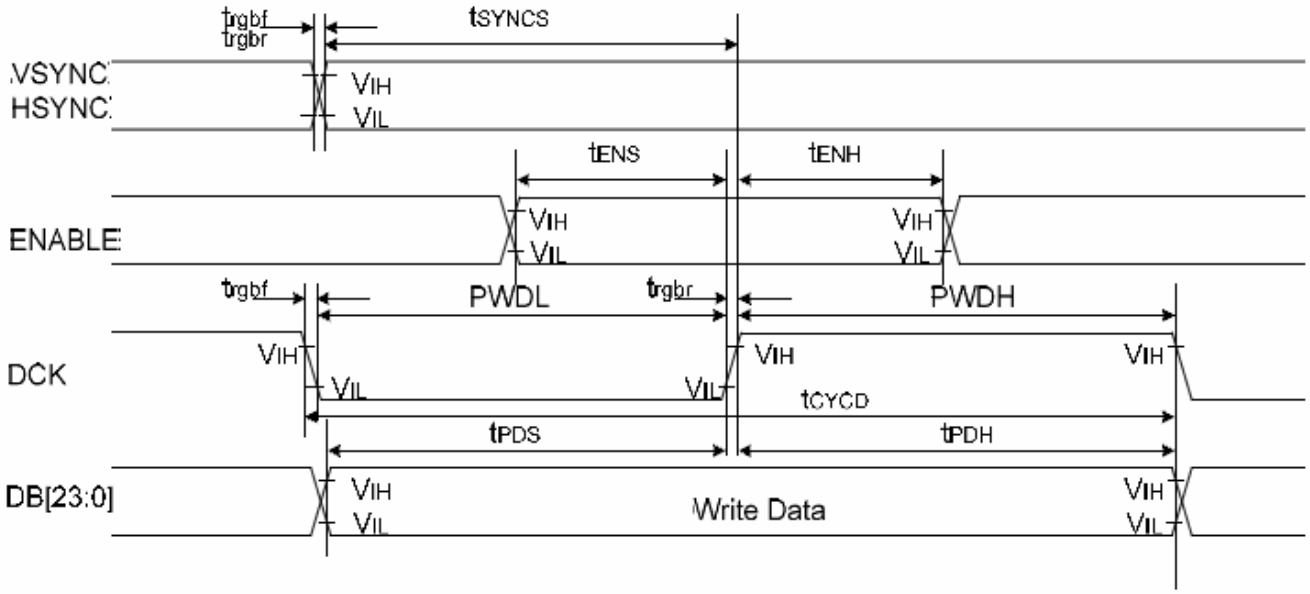


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
DCX	tas	DCX setup time	10	-	ns	
	tah	DCX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA (Output)	tacc	Access time (Read)	10	50	ns	CL = 30pF (maximum)
	toh	Output disable time (Read)	15	50	ns	CL = 8pF (minimum)

Notes:

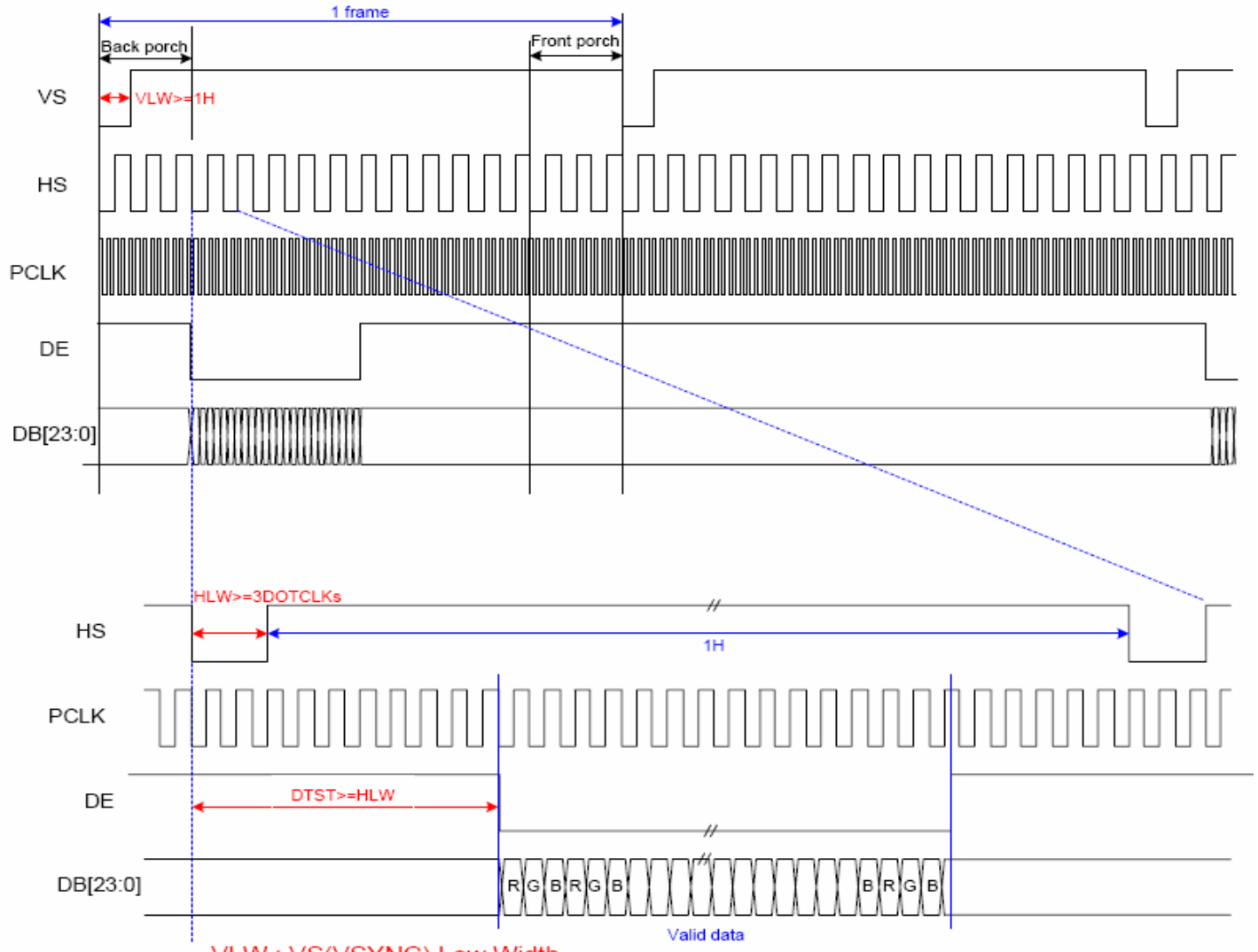
1. Ta = -30 to 70°C, VDDI = 1.65V to 3.3V, VDDA = 2.6V to 4.8V, VSSAM = GND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

6.3 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	5	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	5	-	ns	
	t_{ENH}	ENABLE hold time	5	-	ns	
DB [17:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
DCK	PWDH	DCK high-level period	13	-	ns	
	PWDL	DCK low-level period	13	-	ns	
	t_{CYCD}	DCK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	DCK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70°C, VDDI = 1.65V to 3.3V, VDDA = 2.6V to 4.8V, VSSAM = GND = 0V



VLW : VS(VSYNC) Low Width
HLW : HS(HSYNC) Low Width
DTST : Data Transfer Startup Time

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		50	-	70	fps
Horizontal Low Pulse Width	HLW		5	-	80	DOTCLK
Horizontal Back Porch	HBP		10	-	85	DOTCLK
Horizontal Address	HACT		-	480	-	DOTCLK
Horizontal Front Porch	HFP		5	-	80	DOTCLK
Horizontal Blanking Period	HBP + HFP		60		90	DOTCLK
Vertical Low Pulse Width	VLW		2	-	4	Line
Vertical Back Porch*	VBP		4	-		Line
Vertical Address	VACT		-	864	-	Line
Vertical Front Porch	VFP		2	-		Line
Vertical Blanking Period	VBP + VFP		6			Line
Data Clock	DCLK		23.5	-	34.9	MHz

6.4 Reset Timing Characteristics

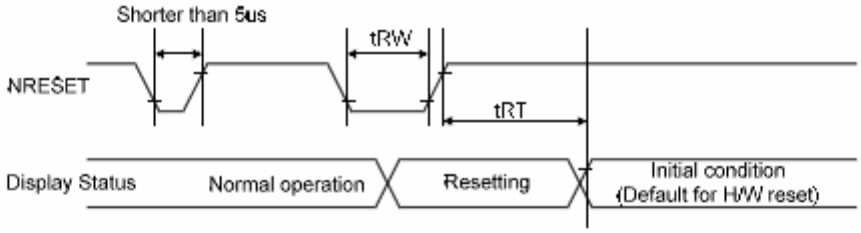


Figure 182: Reset Timing

Table 46: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (note 1,5)	ms
				120 (note 1,6,7)	ms

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. A spike due to an electrostatic discharge on the RESX line does not cause irregular system reset, according to the Table 47.

Table 47: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains blank in the Sleep In mode.), and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse as shown below:

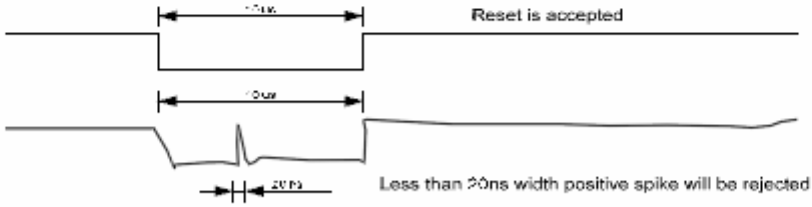


Figure 183: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing the RESX before sending commands. Moreover, the Sleep Out command cannot be sent in 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

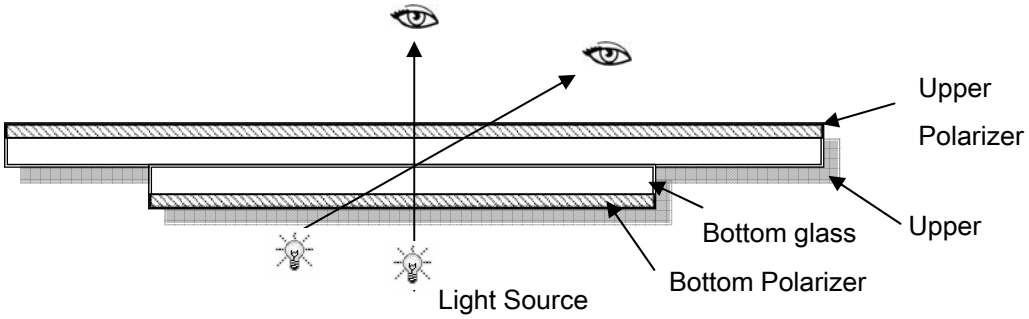
Temperature：25±5℃

Humidity： 65%±10%RH

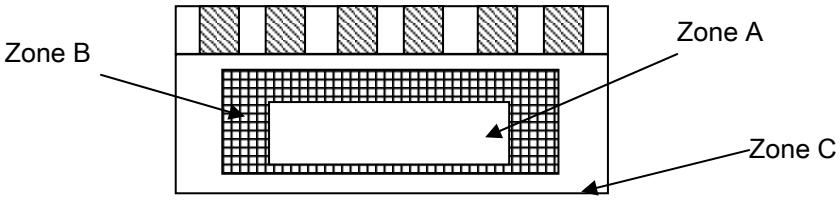
Viewing Angle：Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A：Effective Viewing Area(Character or Digit can be seen)

Zone B：Viewing Area except Zone A

Zone C：Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

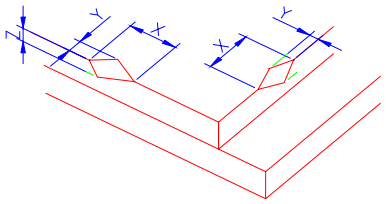
AQL:

Major defect	Minor defect
0.65	1.5

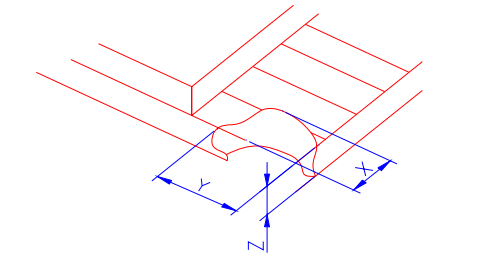
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

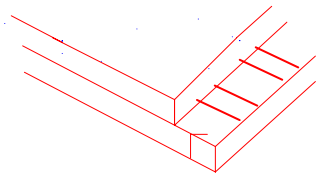
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

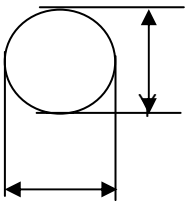
7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)
1.0 LCD Crack/Broken NOTE: X: Length Y: Width	(1) The edge of LCD broken	

X	Y	Z
≤3.0mm	<Inner border line of the seal	≤T

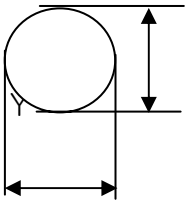
<table>
<tr><td rowspan="2">Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(2)LCD corner broken</td><td> 

<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

<table>
<tr><th>Number</th><th>Items</th><th>Criteria (mm)</th></tr>
<tr><td>2.0</td><td>Spot defect
 
X
Φ=(X+Y)/2</td><td>① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.15</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.15<Φ≤0.2</td><td colspan="2">1</td></tr>
<tr><td>0.2<Φ</td><td colspan="2">0</td></tr>
</table>
②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.2<Φ≤0.3</td><td colspan="2">1</td></tr>
<tr><td>Φ＞0.3</td><td colspan="2">0</td></tr>
</table>
③ Polarizer accidented spot
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<Φ≤0.5</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table></td></tr>
<tr><td></td><td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td><td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table></td></tr>
</table>

Items	Criteria (mm)

Spot defect



X

Φ=(X+Y)/2

① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.15	3(distance≧10mm)		
0.15<Φ≤0.2	1		
0.2<Φ	0		

②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.1<Φ≤0.2	2(distance≧10mm)		
0.2<Φ≤0.3	1		
Φ＞0.3	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

Line defect (LCD/TP /Polarizer black/white line, scratch, stain)

Width(mm)	Length(mm)	Acceptable Qty		
		A	B	C
Φ≤0.03	Ignore	Ignore		Ignore
0.03<W≤0.05	L≤3.0	N≤2		
0.05<W≤0.08	L≤2.0	N≤2		
0.08<W	Define as spot defect			

Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance≧10mm)		
0.4<Φ≤0.6	1		
0.6<Φ	0		

SMT

According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.

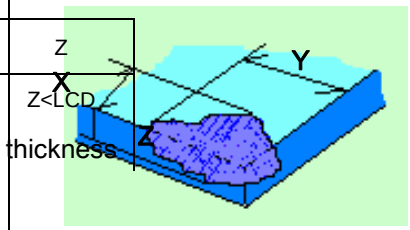
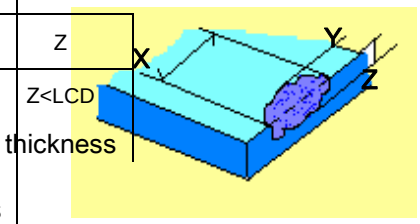
TP bubble/ accidented spot

Size Φ(mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.1<Φ≤0.2	2		
0.2<Φ≤0.3	1		
0.3<Φ	0		

Assembly deflection

beyond the edge of backlight ≤0.15mm

<table>
<tr>
<td rowspan="3">5.0</td>
<td rowspan="3">TP
Related</td>
<td>Newton
Ring</td>
<td>Newton Ring area>1/3 TP area NG

Newton Ring area≤1/3 TP area OK</td>
<td> 
</td>
</tr>
<tr>
<td>TP corner broken
X：length
Y：width
Z：height</td>
<td><table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr>
</table>
* Circuitry broken is not allowed.</td>
<td> 
</td>
</tr>
<tr>
<td>TP edge broken
X：length
Y：width
Z：height</td>
<td><table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thickness</td></tr>
</table>
* Circuitry broken is not allowed.</td>
<td> 
</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	－30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

10.Packing

----TBD----------