



**SPECIFICATION
FOR
LCD Module
KD030C-2-TP**

MODULE:	KD030C-2-TP
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2012.05.29

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		



Revision History

[illegible]

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General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.0" TFT-LCD contains 240x400 pixels, and can display up to 65K/262K colors.

* Features

- Low Input Voltage: 2.8V~3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K colors
- Interface: 8-bits, 9-bits, 16-bits, 18-bits MCU interface.
16-bits, 18-bits RGB interface with graphic controller.
3-line/4-line serial interface.

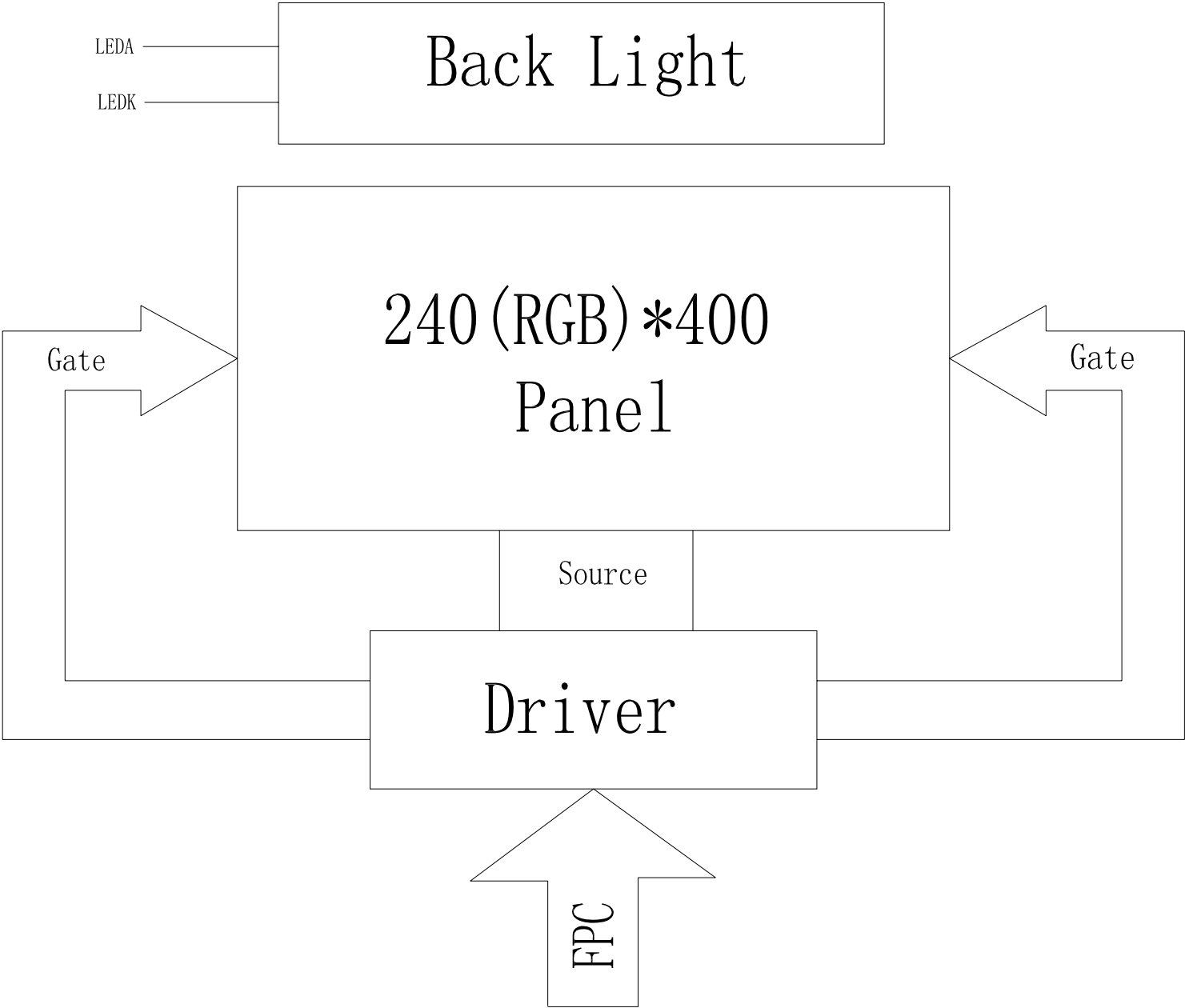
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	38.88(H)*64.80(V) (3.0inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262k	colors	-
Number of pixels	240(RGB)*400	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.051(H)*0.051(V)	mm	-
Viewing angle	12:00	o'clock	-
Controller IC	ILI9327	-	-
Display mode	Transmissive/Normally White	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		45.4		mm	-
	Vertical(V)		77		mm	-
	Depth(D)		3.7		mm	-
Weight			TBD		g	-

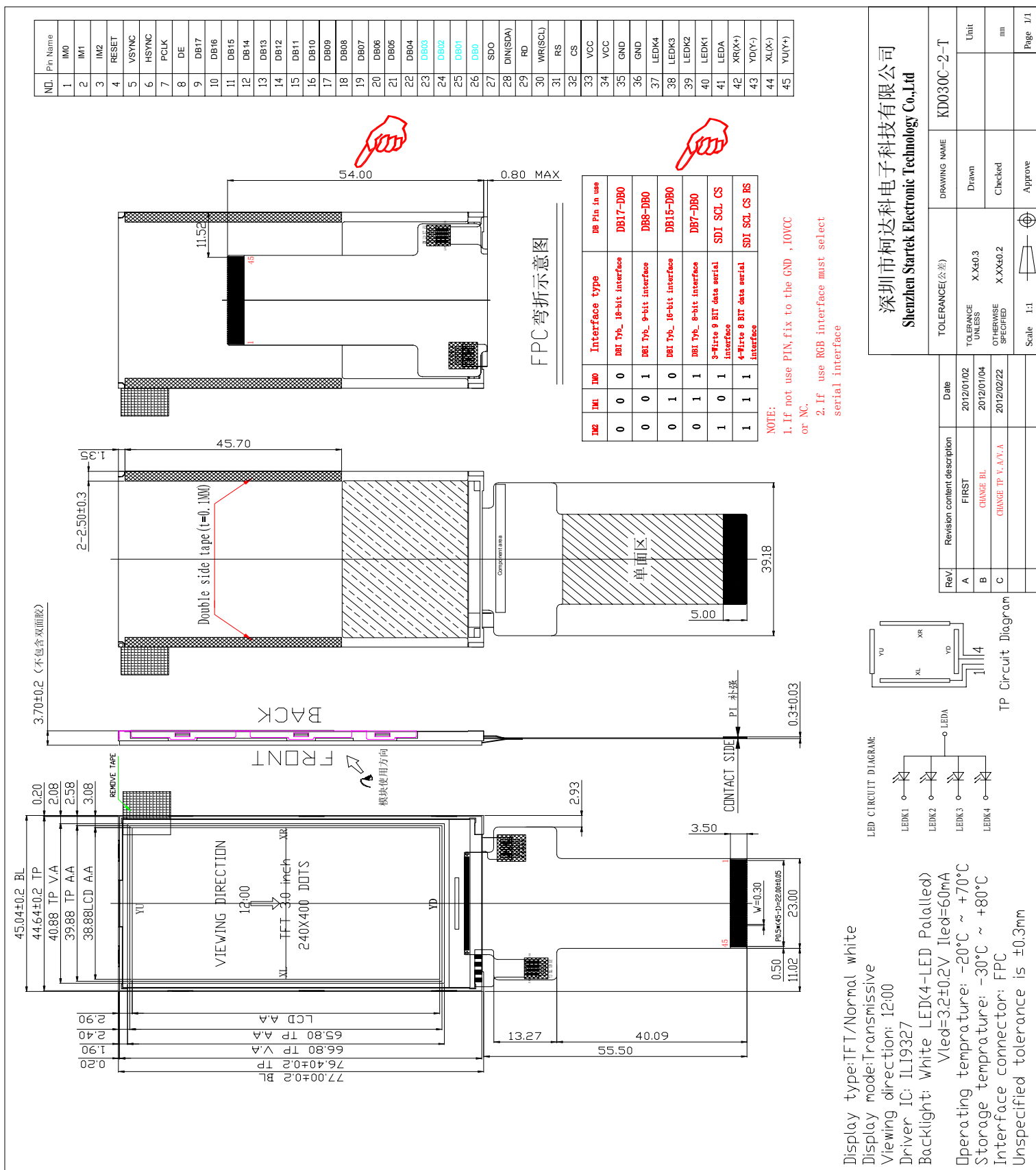


1. Block Diagram





2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	Description	
1	IM0	Interface selecting signal.	I
2	M1		
3	IM2		
4	RESET	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active	I
5	VSYNC	Vertical sync. signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_CS) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
6	HSYNC	Horizontal sync. signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_RS) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
7	PCLK	Pixel clock signal in DPI interface mode. If not used, please fix this pin at GND level.	I
8	DE	Data enable signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_WR) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
9-26	DB17-DB0	These pins are data bus. In MDDI operation, DB[17:9]/S_DB[8:0] can be assigned for the sub-display interface output. In MDDI mode, these pins are output, If they are not used; please let these pins as open. In other mode, these pins are input, If they are not used; please fix these pins as GND.	I/O
27	SDO	Serial data output pin and used for the DBI type C mode.	O
28	DIN	Serial data input pin and used for the DBI type C mode. If not used, please connect this pin to ground.	I

29	RD	Read control pin for the DBI interface. If not used, please connect this pin to VCC.	I
30	WR(SCL)	Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to VCC.	I
31	RS	Display data / Command selection pin D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.	I
32	CS	Chip select input pin ("Low" enable). When it is not used, please fix this pin at VCC.	I
33	VCC	Power supply voltage(VCI=2.5V-3.3V).	P
34	VCC		
35	GND	Ground.	P
36	GND		
37	LEDK4	LED Cathode 4.	P
38	LEDK3	LED Cathode 3.	P
39	LEDK2	LED Cathode 2.	P
40	LEDK1	LED Cathode 1.	P
41	LEDA	LED Anode.	P
42	XR(NC)	NC.	
43	YD(NC)	NC.	
44	XL(NC)	NC.	
45	YU(NC)	NC.	

4. LCD Optical Characteristics

4.1 Optical specification

(Note1・Note2)
(Using CPT LC+ EWV Polarizer+Corresponding Backlight, reference only)

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Transmittance		T		(5.2)	(5.5)		%	
Contrast Ratio		CR	*1)		(250)	-	--	Note 3
Response Time		Tr+ Tf	*3)	-	(30)		ms	Note 4
Viewing Angle	Vertical	θ *2)	$CR \geq 10$	(100)	(110)	-		
						-		Note 5
	Horizontal	ϕ *2)		(120)	(130)	-		
						-		
Color Filter Chromaticity	White	x y Y	$\theta = \phi = 0^\circ$	(0.288)	(0.308)	(0.328)		Note 6
				(0.322)	(0.342)	(0.362)		
				(27.8)	(30.8)	(33.8)		
	Red	x y Y	$\theta = \phi = 0^\circ$	(0.633)	(0.653)	(0.673)		
				(0.311)	(0.331)	(0.351)		
				(15.4)	(18.4)	(21.4)		
	Green	x y Y	$\theta = \phi = 0^\circ$	(0.291)	(0.311)	(0.331)		
				(0.554)	(0.574)	(0.594)		
				(55.0)	(59.0)	(63)		
	Blue	x y Y	$\theta = \phi = 0^\circ$	(0.114)	(0.134)	(0.154)		
				(0.114)	(0.134)	(0.154)		
				(12.3)	(15.3)	(18.3)		
	NTSC				-	(61%)	-	

4.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2℃
- 15min. warm-up time

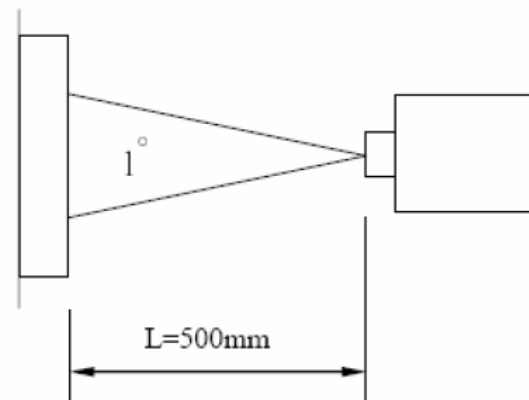
4.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.



Note 1. Ambient condition : $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$, $60 \pm 10\% \text{RH}$, under 10 Lux in the darkroom .

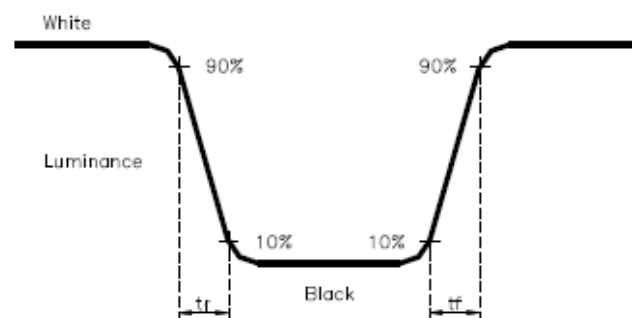
Note 2. Measure device : BM-5A (TOPCON) , viewing cone= 1° , $I_L=20\text{mA}$.



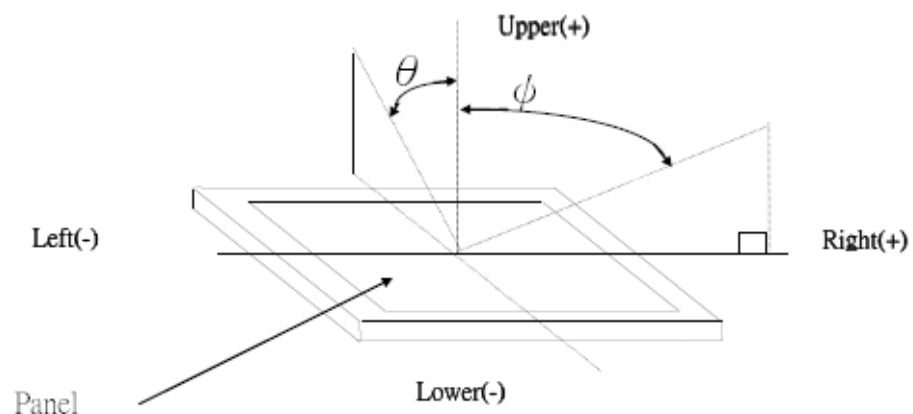
Note 3. Definition of Contrast Ratio :

$$\text{CR} = \text{White Luminance (ON)} / \text{Black Luminance (OFF)}$$

Note 4. Definition of response time : The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle(θ , ψ) :



Note 6. Light source: C light.

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5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

5.2 DC Electrical Characteristics

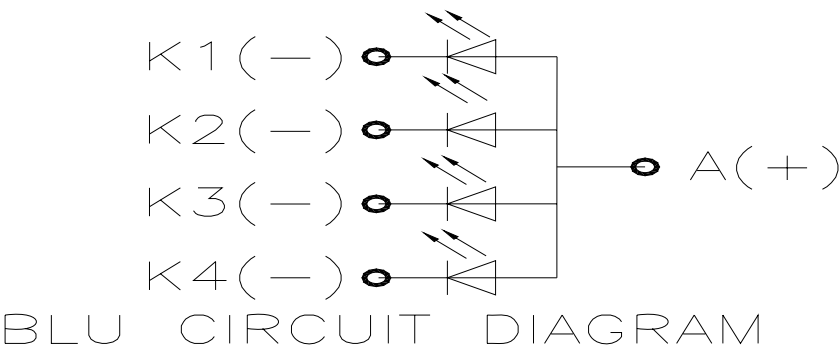
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.6	3.3	4.2	V	
Digital interface supply Voltage	VDDIO	1.65	3.3	4.2	V	
Normal mode Current consumption	IDD	--	10	--	mA	
Level input voltage	V _{IH}	0.7V _{DDIO}		VDDIO	V	
	V _{IL}	GND		0.3V _{DDIO}	V	
Level output voltage	V _{OH}	0.8VDDIO		VDDIO	V	
	V _{OL}	GND		0.2VDDIO	V	



5.3 LED Backlight Characteristics

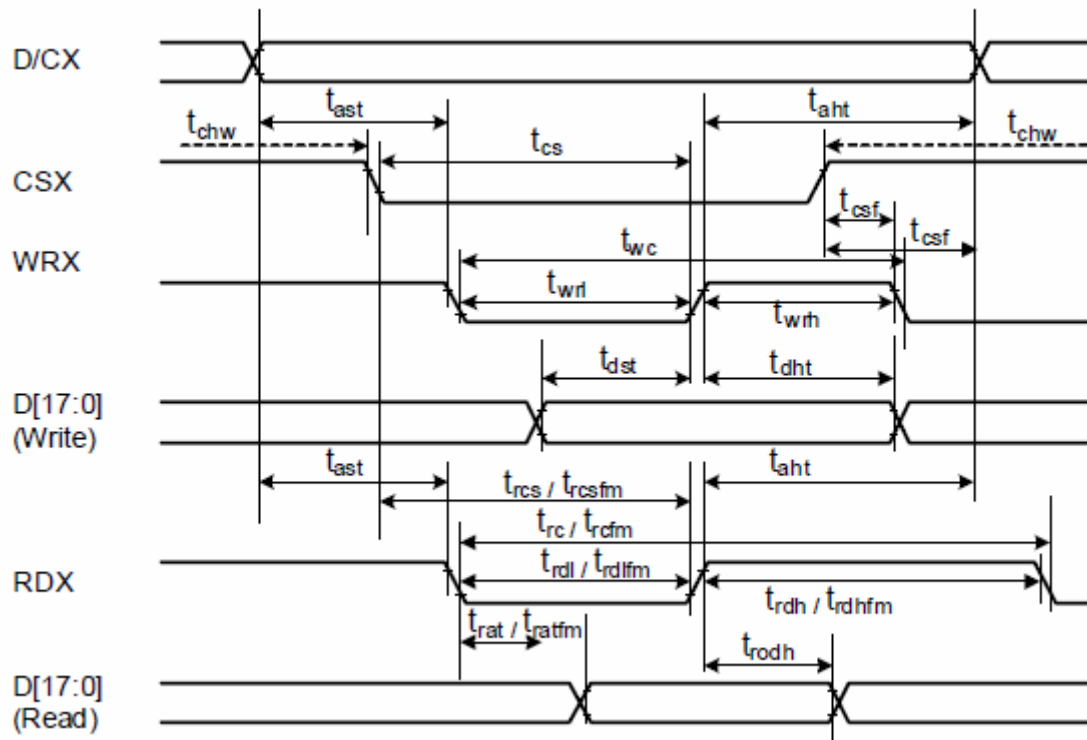
The back-light system is edge-lighting type with 4chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	60	80	--	mA	
Forward Voltage	V_F	2.9	3.2	3.4	V	
LCM Luminance	L_V	300	--	--	cd/m2	$I_F=80mA$
Uniformity	AV_g	80	--	--	%	-



6. AC Characteristic

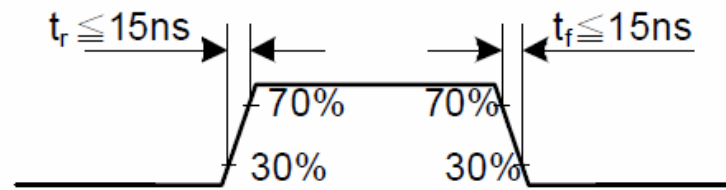
6.1 DBI Type B (18/16/9/8 bit) Interface Timing Characteristics



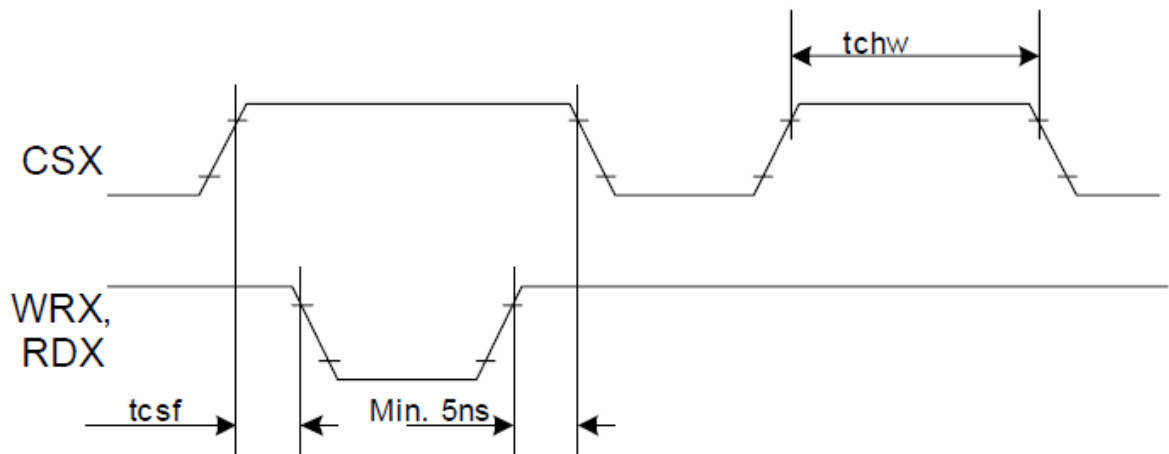
Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	10	-	ns	
CSX	t _{chw}	CSX "H" Pulse Width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	20	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{twc}	Write cycle	80	-	ns	
	t _{twrh}	Write Control pulse H duration	25	-	ns	
	t _{twrl}	Write Control pulse L duration	25	-	ns	
RDX (ID)	t _{trc}	Read cycle (ID)	160	-	ns	
	t _{trdh}	Read Control pulse H duration (ID)	90	-	ns	
	t _{trdl}	Read Control pulse L duration (ID)	45	-	ns	
RDX (FM)	t _{trcfm}	Read cycle (FM)	450	-	ns	
	t _{trdhfm}	Read Control pulse H duration (FM)	90	-	ns	
	t _{trdlfm}	Read Control pulse L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	t _{dst}	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Data hold time	10	-	ns	
	t _{rat}	Read access time (ID)	-	40	ns	
	t _{ratfm}	Read access time (FM)	-	340	ns	
	t _{odh}	Output disable time	20	-	ns	



Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{DD}=2.5\text{V}$ to 3.0V , $DGND=0\text{V}$

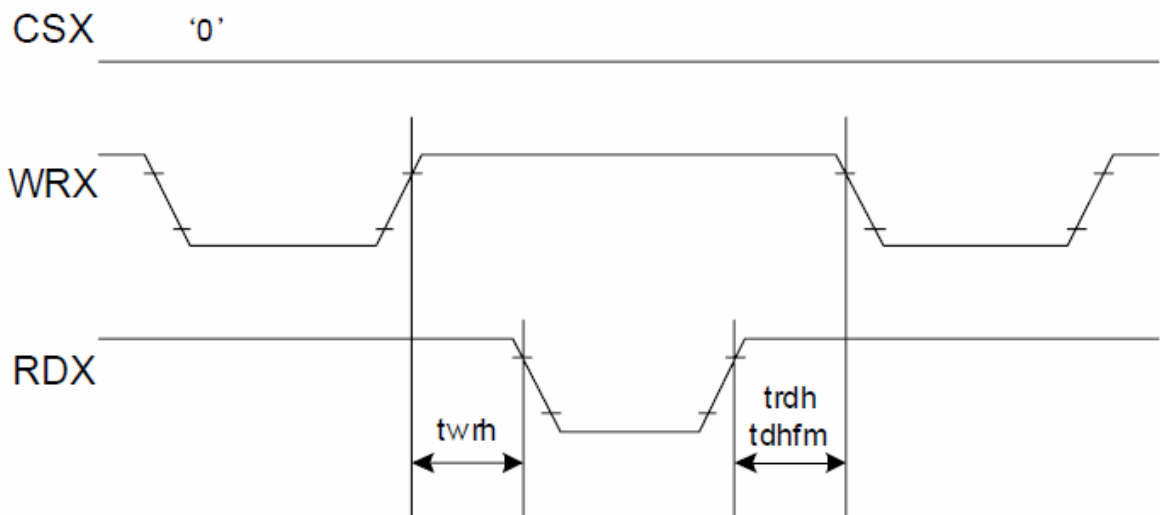


CSX timings:



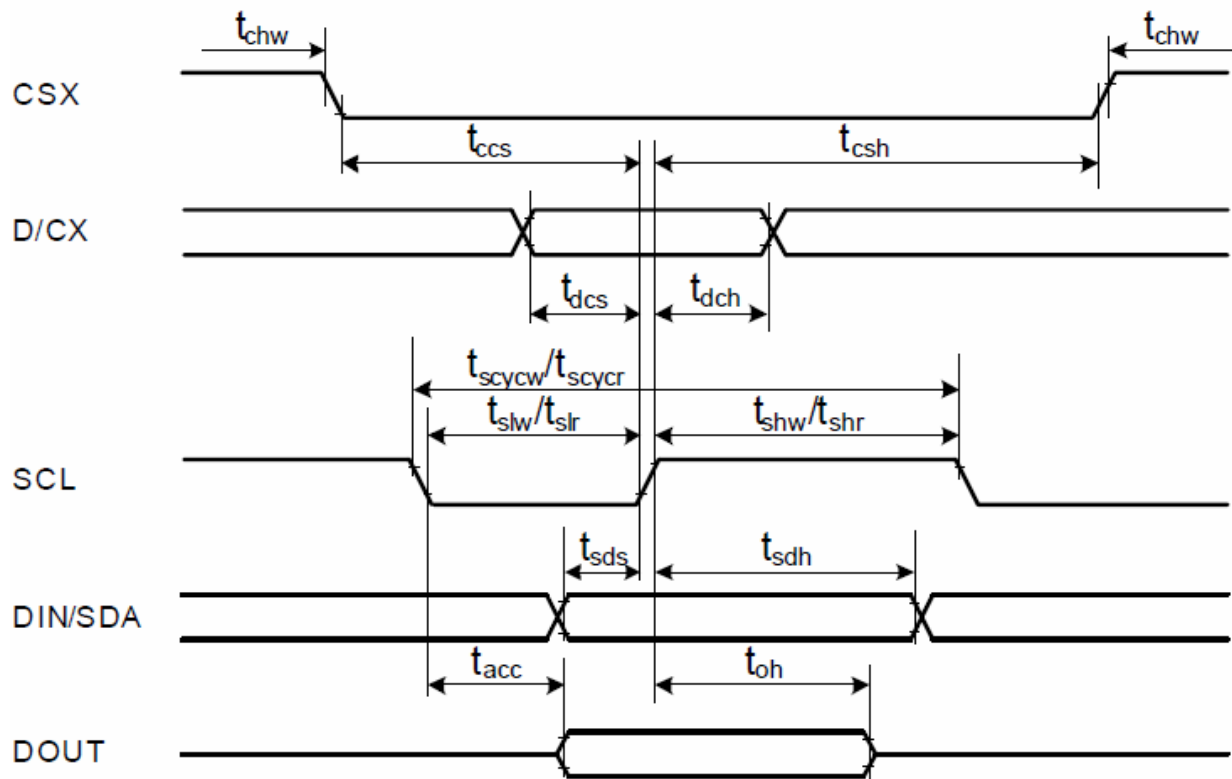
Note: Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

Write to read or read to write timings:



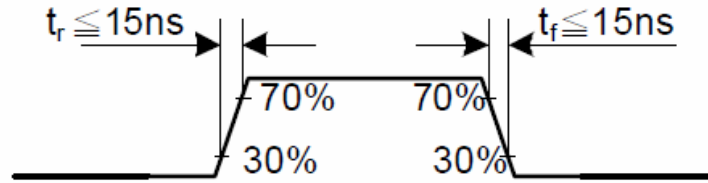
Note: Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

6.2 DBI Type C (SPI) Interface Timing Characteristics

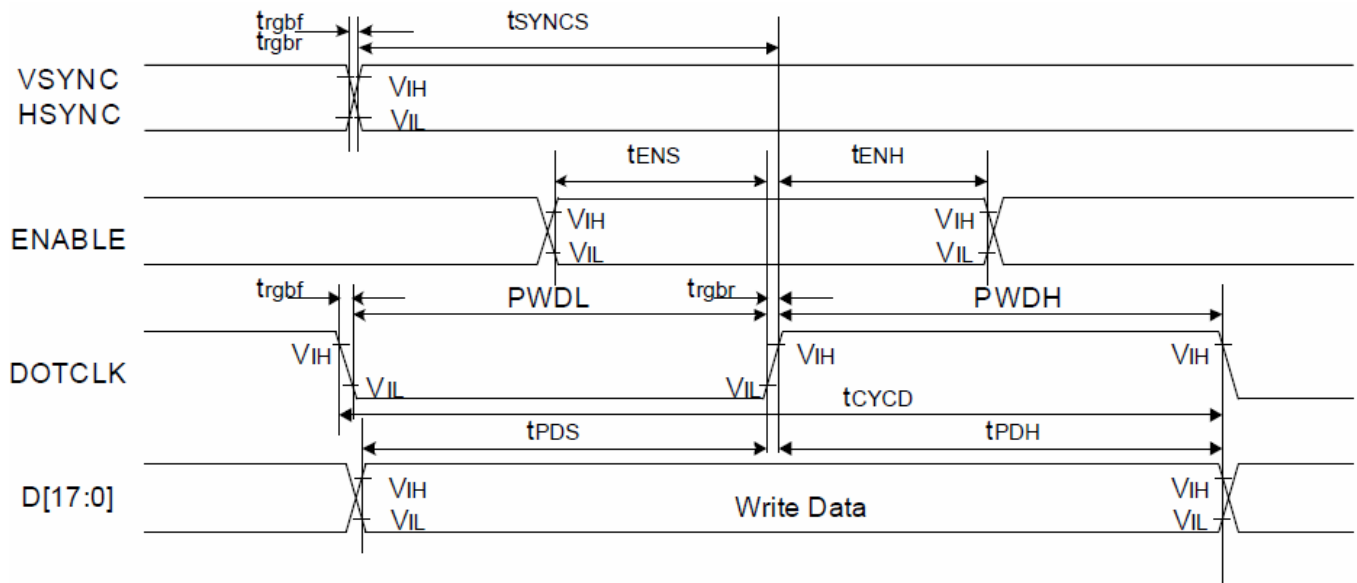


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	CSX-SCL time (Write)	15	-	ns	
	t_{csh}	CSX-SCL time (Write)	15	-	ns	
	t_{css}	CSX-SCL time (Read)	60	-	ns	
	t_{csh}	CSX-SCL time (Read)	60	-	ns	
	t_{chw}	CSX "H" pulse time	40	-	ns	
SCL	t_{scycw}	Serial clock cycle (Write)	60	-	ns	
	t_{shw}	SCL "H" pulse width (Write)	15	-	ns	
	t_{slw}	SCL "L" pulse width (Write)	15	-	ns	
	t_{scycr}	Serial clock cycle (Read GRAM)	300	-	ns	
	t_{shr}	SCL "H" pulse width (Read GRAM)	110	-	ns	
	t_{slr}	SCL "L" pulse width (Read GRAM)	110	-	ns	
	t_{scycr}	Serial clock cycle (Read ID)	150	-	ns	
	t_{shr}	SCL "H" pulse width (Read GRAM)	54	-	ns	
	t_{slr}	SCL "L" pulse width (Read GRAM)	54	-	ns	
D/CX	t_{dcs}	D/CX setup time	7	-	ns	
	t_{dch}	D/CX hold time	7	-	ns	
SDA (Input) (Output)	t_{acc}	Access time	10	50	ns	For maximum CL=30pF
	t_{oh}	Output disable time	15	50	ns	For minimum CL=8pF
	t_{sds}	Data setup time	7	-		
	t_{sdh}	Data hold time	7	-		

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{DD}=2.5\text{V}$ to 3.0V , $AGND=DGND=0\text{V}$



6.3 RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{synCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{synCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
	$PWDH$	DOTCLK high-level period	15	-	ns	
	$PWDL$	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{synCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{synCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	$PWDH$	DOTCLK high-level pulse period	15	-	ns	
	$PWDL$	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

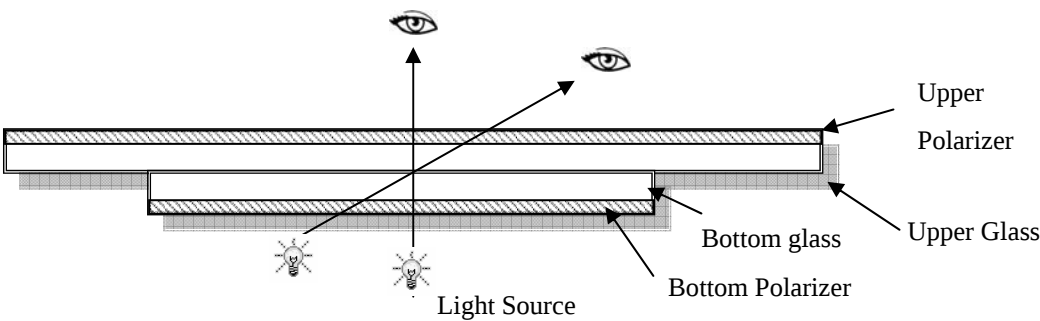
7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

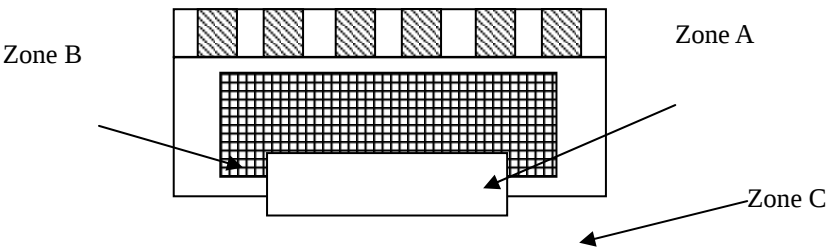
7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



7.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

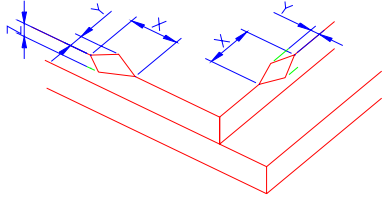
AQL:

Major defect	Minor defect
0.65	1.5

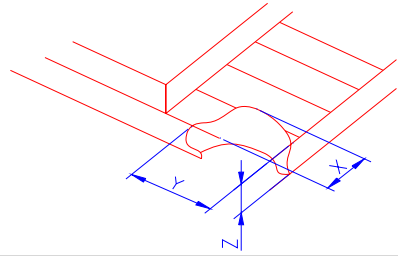
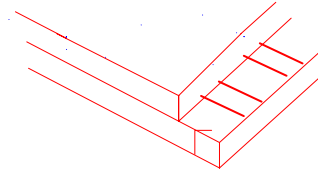
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken	(1) The edge of LCD broken	 <table> <tr> <th>X</th><th>Y</th><th>Z</th></tr> <tr> <td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
NOTE: X: Length Y: Width Z: Height L: Length of ITO,								



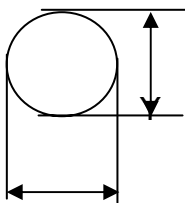
T: Height of LCD	(2)LCD corner broken	 <table border="1" data-bbox="914 546 1327 647"><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T
	X	Y	Z					
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

Number	Items	Criteria (mm)
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2.0

Spot defect



X

$$\Phi = (X + Y) / 2$$

① light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.10$	Ignore		Ignore
$0.10 < \Phi \leq 0.15$	3(distance $\geq 10\text{mm}$)		
$0.15 < \Phi \leq 0.2$	1		
$0.2 < \Phi$	0		

② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		Ignore
$0.1 < \Phi \leq 0.2$	2(distance $\geq 10\text{mm}$)		
$0.2 < \Phi \leq 0.3$	1		
$\Phi > 0.3$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	0		

Line defect
(LCD/TP
/Polarizer
black/white
line, scratch,
stain)

Width(mm)	Length(mm)	Acceptable Qty		
		A	B	C
$\Phi\leq0.03$	Ignore	Ignore		Ignore
$0.03<W\leq0.05$	$L\leq3.0$	$N\leq2$		
$0.05<W\leq0.08$	$L\leq2.0$	$N\leq2$		
$0.08<W$	Define as spot defect			

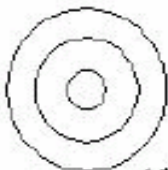
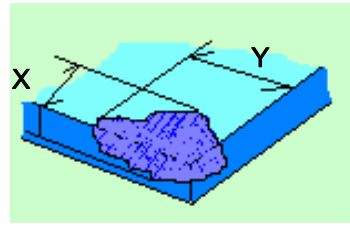
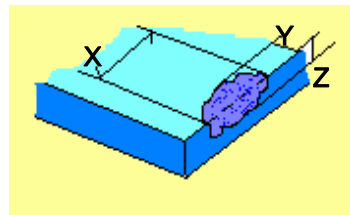


Items	Criteria (mm)
Spot defect	</



	Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.03$</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>$0.03<W\leq0.05$</td><td>$L\leq3.0$</td><td colspan="2">$N\leq2$</td></tr><tr><td>$0.05<W\leq0.08$</td><td>$L\leq2.0$</td><td colspan="2">$N\leq2$</td></tr><tr><td>$0.08<W$</td><td colspan="4">Define as spot defect</td></tr></table>					Width(mm)	Length(mm)	Acceptable Qty			A	B	C	$\Phi\leq0.03$	Ignore	Ignore		Ignore	$0.03<W\leq0.05$	$L\leq3.0$	$N\leq2$		$0.05<W\leq0.08$	$L\leq2.0$	$N\leq2$		$0.08<W$	Define as spot defect			
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	Polarizer Bubble	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.2$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.2<\Phi\leq0.4$</td><td colspan="2">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.4<\Phi\leq0.6$</td><td colspan="2">1</td></tr><tr><td>$0.6<\Phi$</td><td colspan="2">0</td></tr></table>					Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.2$	Ignore		Ignore	$0.2<\Phi\leq0.4$	2(distance $\geq 10\text{mm}$)		$0.4<\Phi\leq0.6$	1		$0.6<\Phi$	0							
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	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																														
		TP bubble/ accidented spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.1$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.1<\Phi\leq0.2$</td><td colspan="2">2 (distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.2<\Phi\leq0.3$</td><td colspan="2">1</td></tr><tr><td>$0.3<\Phi$</td><td colspan="2">0</td></tr></table>				Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.1$	Ignore		Ignore	$0.1<\Phi\leq0.2$	2 (distance $\geq 10\text{mm}$)		$0.2<\Phi\leq0.3$	1		$0.3<\Phi$	0							
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		Assembly deflection	beyond the edge of backlight $\leq0.15\text{mm}$																													



5.0	TP Related				 1 规律性						
		Newton Ring	Newton Ring area>1/3 TP area Newton Ring area≤1/3 TP area	NG OK	 2 非规律性						
					 似牛顿环						
		TP corner broken X : length Y : width Z : height	<table border="1"><thead><tr><th>X</th><th>Y</th><th>Z</th></tr></thead><tbody><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr></tbody></table> * Circuitry broken is not allowed.	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thickness		
X	Y	Z									
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X	Y	Z									
X≤6.0mm	Y≤2.0mm	Z<LCD thickness									



Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	60℃, 90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	- 30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10.Packing

---TBD----

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